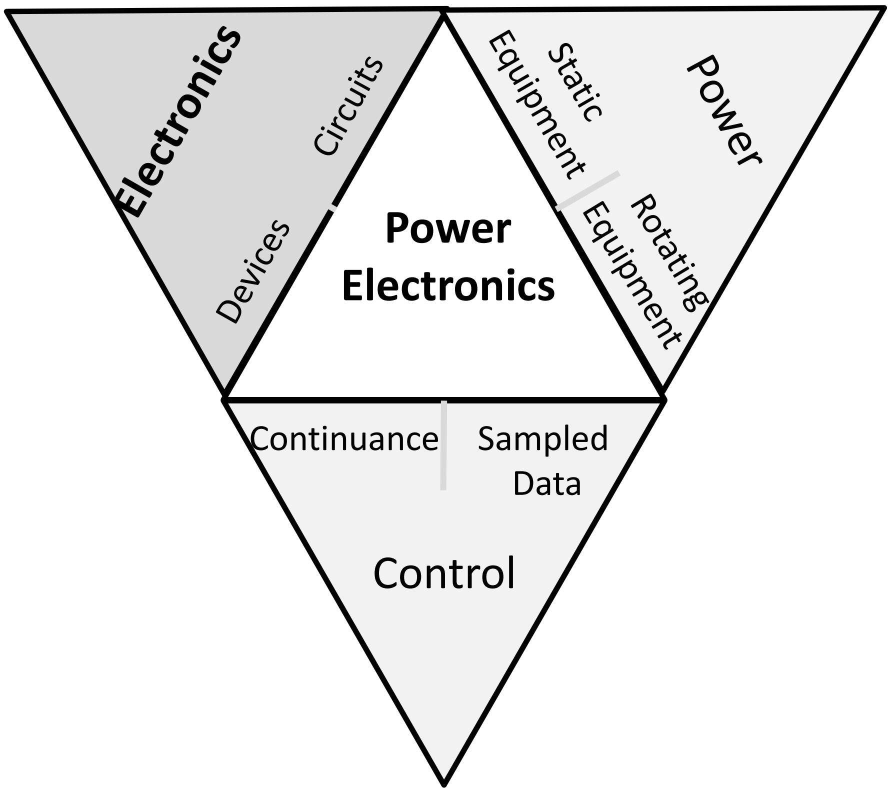
SIMetrix/SIMPLIS Simulation for Power Electronics

Contents

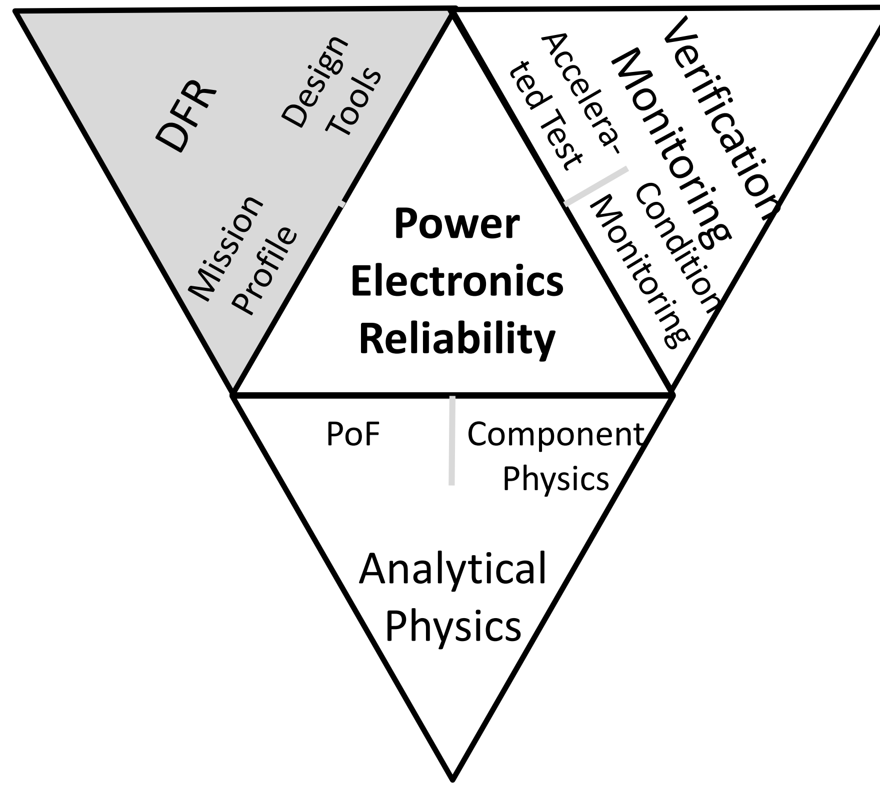
1. PE(Power Electronics) and Simulation
2. SIMetrix/SIMPLIS 특징
3. Components SPICE/PWL Model
4. PE Example

intergratech™

1-1 Scope of Power Electronics and Reliability



Power Electronics
by William E.Newell in 1970

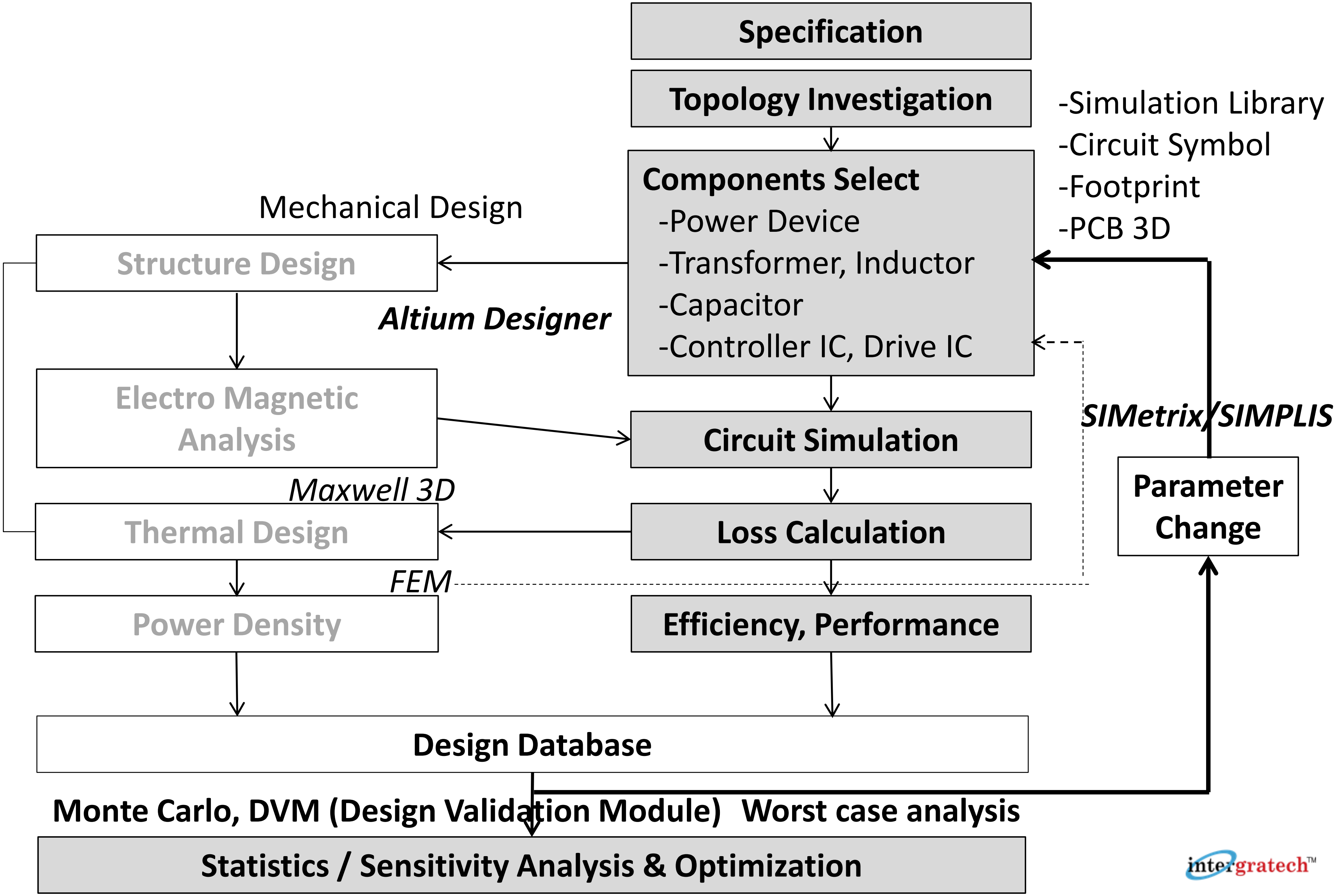


Power Electronics Reliability
by CORPE in 2010

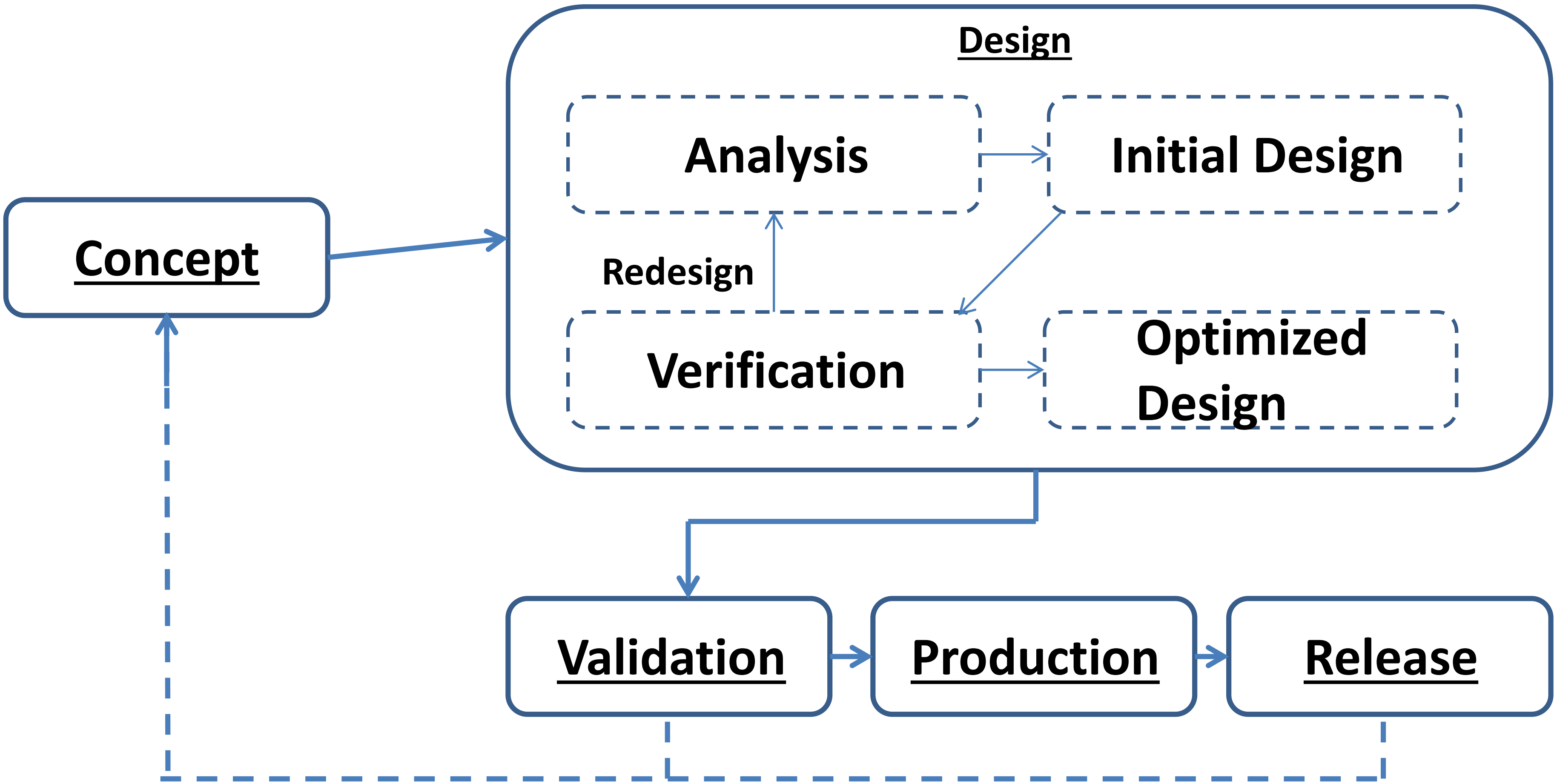
The center addresses a better understanding of how the reliability of power electronic devices and systems is influenced by different stress factors such as **temperature**, **overvoltage** and **current**, and **overload** and **environment**.

intergratech™

1-2 High Quality PE Design Flow



1-3 State of Reliability Design Procedure for Power Electronics Systems

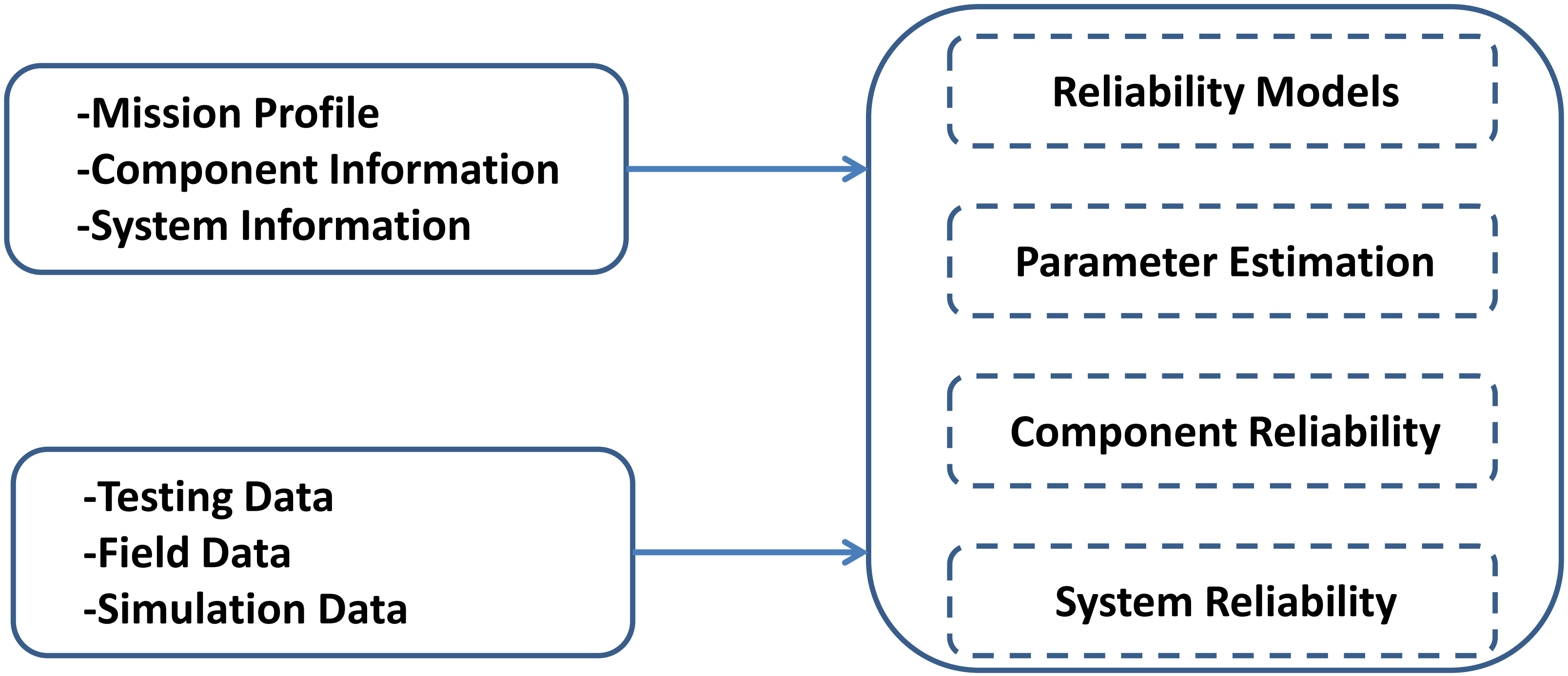


Reference: IEEE INDUSTRIAL ELECTRONICS MAGAZINE JUNE 2013

intergratech™

1-4 High Quality Design Methods

-Safety factors / derating, -worst-case analysis
-Six sigma design, -Statistical design of experiments
-Taguchi design approach
design approach tests the effect of variability of both control factors and noise factors



Reference: IEEE INDUSTRIAL ELECTRONICS MAGAZINE JUNE 2013

Contents

intergratech™

2-1 PE회로 해석에 적용한 Simulator 종류

Simulator	EMTP	SPICE	SABER	**SIMPLIS**	SCAT	KREAN	PSIM	SIMPROLA	MATLAB/ SIMILINK
수치적분법	Trapezoidal	Trapezoidal (Default), Gear	Gear (Default), Trapezoidal	선이행열 급수전개 근사법	Trapezoidal	Semi-implicit Runge-Kutta	Trapezoidal	-	Runge-Kutta (Default)
회로 정식화	절점해석	수정절점해 석	수정접점해 석	상태변수해 석	상태변수해 석	상태변수해 석	절점해석	절점해석	상태변수해 석
계산Step	Fix(지정)	Variable (자동)	Variable (자동)	Variable (자동)	Variable (자동)	Variable (자동)	Fix(자동)	Variable	Fix/Variable 선택 가
계산Step	Ideal switch	Ideal / Non lineal / 소자 모델링	Ideal / Non li neal / 소자 모델링	Ideal / Non li neal / 소자 모델링	Ideal	Ideal	Ideal	Ideal	Ideal
Switch시의 취급	영점보상 없음	오차평가가 수속할때까 지 Step을 재계산	전후값으로 보간	전후값으로 보간	Newton법과 2분법	전후값으로 보간	영점보상 없음	-	없음
개발목적	계통Surge 해석	집적회로 설계	시스템 설계	Switching 전원설계	Switching 전원설계	PE회로	PE회로	PE회로	제어계 설계
분야	회전기 /계통 해석	소자모델 포함 상세한 해석	기계/열계 등과 연동 해석	同上	同上	Motor제어	同上	Magnetics/F EA 해석과 연동 가능	同上
그외	-	User가 많고 교육용서적 풍부	MAST언어 로 모델구축가 능 SPICE호완 Lib 있음	주기정상상 태 / 주파수해석 이 가능	주기정상상 태/주파수 해석이 가능	-	PE model LIB있음	ANSIS가 제공하는 Simulator module로 시스템 구축 용이	Power System Blockset 로 support

intergratech™

2-2 Switching Mode PE향 Simulator

-Switching 회로를 고속으로 Simulation 가
-SIMPLIS
    -1989 Duke대학교에서 AT&T향으로 개발. 현재는 Transim
        SPICE계SIMetrix와 통합한 SIMetrix/SIMPLIS
        SIMPLIS->System Level를 고속으로, SIMetrix->고정도
        Switching회로를 포함한 System의 AC 해석이 가능
-SCAT
    -1992 Shojo대학교 Nakahara교수 개발
    -Switching전원 해석/설계용
-PSIM
    -1995 British Columbia대학교(Canada)에서 개발
    -PE용. 전자계Soft JMAG와 연성가능

-System의 Hybrid성, -System의 Nonlinear성
-Switching의 문제, -Stiff

intergratech™

http://www.simplistechnologies.com/

http://www.simetrix.co.uk/site/index.html

http://www.igtech.co.kr/

When SIMPLIS? When Spice?

- Spice is optimized for:
  - Circuits that can be linearized around a DC operating point
    - e.g. Op amp circuits, …
  - IC circuits where Spice models can relate device parameters to process parameters

- SIMPLIS is optimized for switching systems that have:
  - Very fast switching transients and relatively large amounts of energy storage
    - e.g. Closed-loop switching power supplies, Switched capacitor filters, Phase-Locked Loops

SIMPLIS makes Virtual Prototyping Feasible

- For closed-loop switching power supplies,
  - **Vastly superior speed** for transient simulations
    - Typically 10X to 50X faster than Spice
  - **Vastly superior convergence** properties
    - Convergence ceases to be an ever-present concern
  - Ability to quickly find **steady-state** and do **AC analysis** for circuits that have a stable steady-state limit cycle using only the large signal time-domain model – ***no derivation of an average model required***

… make Virtual Prototyping Feasible

2-3 SIMetrix/SIMPLIS 기능

SIMPLIS 의 Simulator 기능

-Transient Analysis (TX) : Transient Waveform

-Periodic Operating Point (POP) : Stead State Waveform

-Frequency Analysis (FX) : Bode Diagram

-SIMetrix의 Simulator 기능

-Transient, -AC Analysis, -DC Sweep, -Noise Analysis

-Transfer function, -Monte Carlo Analysis, -Pole-zero Analysis

-Verilog Co-Simulation

-Analog Circuit와 Verilog-A 및 Verilog-HDL의 Co-Simulation 지원

-Script Edit

-DVM(Design Validation Module)

-SystemDesigner(Support Piccolo)

intergratech™

2-4 PE에 대한 Simulator측의 대책

-Switching 회로 문제의 대책

- -Switching Device Model 의 Level선택(1,2,3)
- -엄밀한 Dynamic Model -> 상태평균화Model
- -회로정식화범의 선택
  - -SPICE : 수정절점해석
  - -SIMPLIS : 상태변수해석
- -수치적분법의 적정화
  - -Tapezoidal
  - -Gear-2
- -계산알고즘 개량

Transim
leading online design.

News & Events

www.transim.com

2014-2-4 MOSFET Selection was never so easy with Toshiba's Web Simulator

2014-1-6 Jumpstart Board Design with GE's Power Module Wizard

2013-11-7 Fairchild's Power Supply WebDesigner Enhanced with Power Train Discrete Device Power Loss and Efficiency Analysis Tools

About Transim

Transim Technology Corporation is the global leader in delivering innovative cloud application engineering solutions for online design support in the electronics industry.

Learn More>>

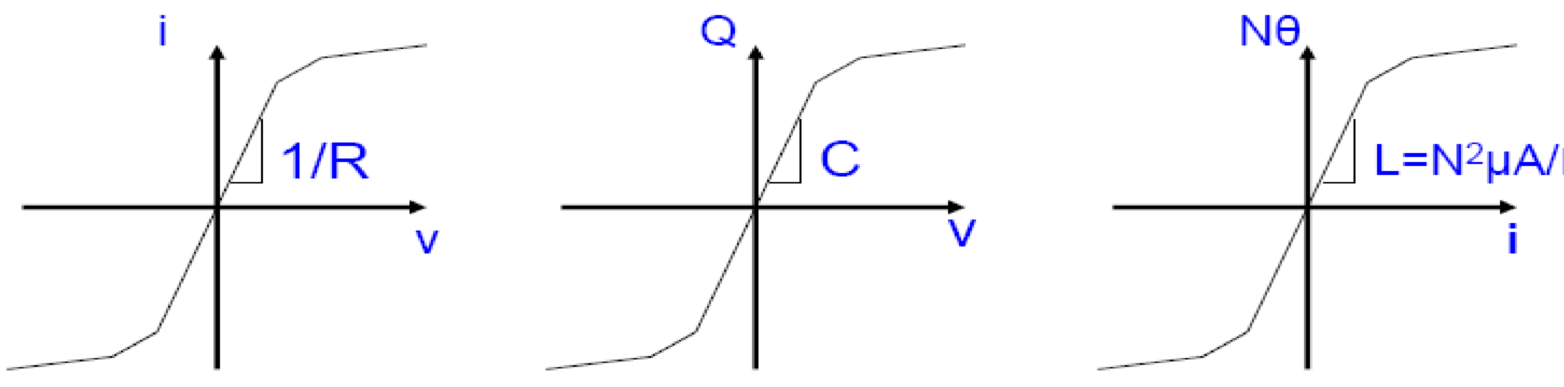
Who's using Transim?

Contents

intergratech™

3-1 Main Components of Power Electronics

Item		Parameters
Switching Device	Ideal Device	Ron=0, Roff=∞, Von=0, Tsw=0, Cpar=0, Lpar=0
	Diode	Vf=0.3V ～ 2V
	MOSFET	1mΩ～10ΩΩ, Vds=10V～1500V
	IGBT	Von=1.3V～3V, Vces=200V～1700V
Energy Storage Device	Inductor L	1/2LI^2
	Capacitor C	1/2CV^2
Lose Device	Resistance R	RI^2
Control Device	IC	Amp, Drive, DSP, FPGA, ASIC…



Piecewise Linear Components (SIMPLIS)

3-2. Device Model

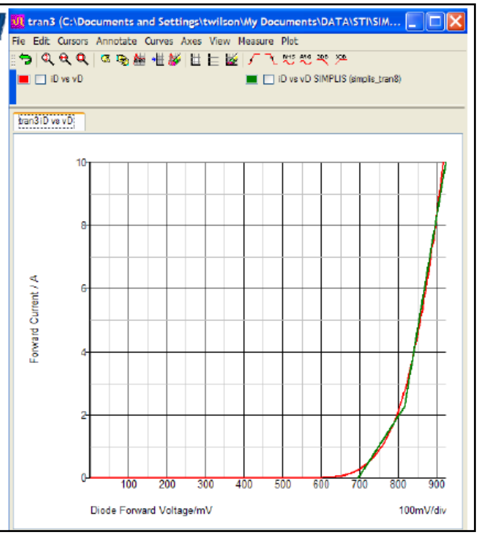
-Device Model(SPICE Model)
전자부품(반도체부품, 수동부품등)의 전기적 거동 표현
-SIMetrix의 Device Model는 SPICE기술.
-SIMetrix/SIMPLIS 의 Components는 크게 두가지
-Genric Components
RCL, DC/AC Source, ADC, DAC, Digital Generic등
-수식모델
Non-liner Transfer Function, Laplace Transfer Function

Multi Level Modeling(SIMPLIS)
Level 1 : Ideal
Level 2 : Stability Analysis
Level 3 : High di/dt Load Transient

3-3. Device Model

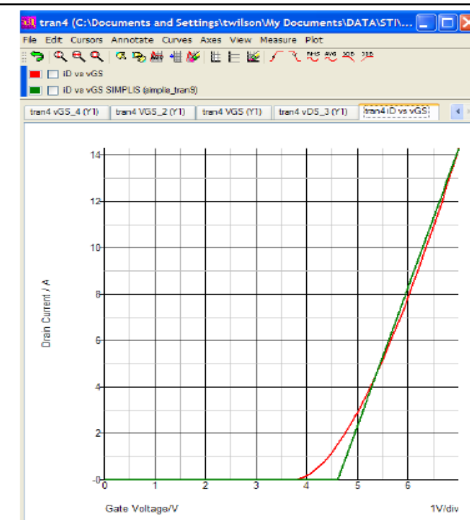
Diode PWL Model

- Three-segment SIMPLIS diode model (green)
- Compared to Spice model (red)
- Fit optimized over 4A – 8A range

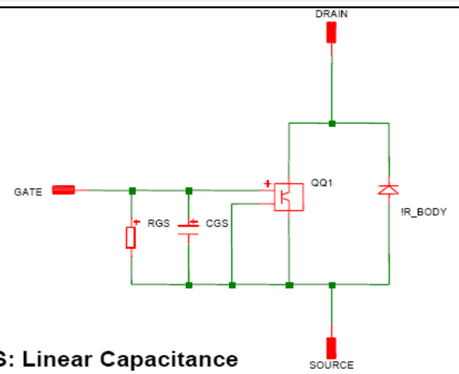


FET PWL Model

- Two-segment SIMPLIS iD vs. vGS (green)
- Compared to Spice model (red)
- Fit optimized over 33% - 100% of Imax

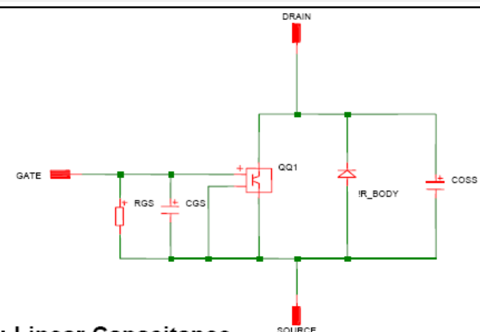


N –Channel MOSFET SIMPLIS Model



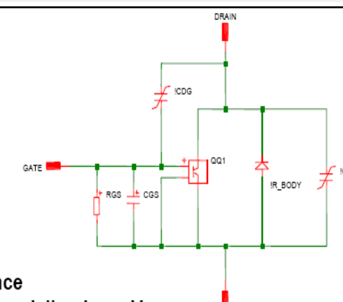
CGS: Linear Capacitance
QQ1: Switch with On & Off Resistance
IR_BODY: Body diode modeled by PWL Resistor

Level 1



CGS: Linear Capacitance
QQ1: Switch with On & Off Resistance
IR_BODY: Body diode modeled by PWL Resistor
COSS: Lumped linear output capacitance

Level 2



CGS: Linear Capacitance
QQ1: SIMPLIS Switch modeling I_d vs. V_{ds} proportional to voltage exceeding VTO
IR_BODY: Body diode modeled by PWL Resistor
!CDG : PWL capacitance
!CDS : PWL capacitance

Level 3

intergratech™

Reference: http://www.simplistechnologies.com/documentation/simplis/installing-simetrix-spice-fet-models

Model Accuracy

- **Accuracy of Physics:** the Physics behind the equations that describe semiconductors
  - Spice - very accurate
  - SIMPLIS – piecewise linear behavioral approximations
- **Accuracy of Parameters:** the value of the constants used in the model
  - Spice – mere mortals cannot typically create their own Spice models
  - SIMPLIS – models are based on data sheet info and can be created by average user in ~20 minutes
- **Accuracy of solution of circuit equations:**
  - Spice – in order to get practical speed, Spice must accept more numerical error (RelTol) per computational step
  - SIMPLIS – takes advantage of piecewise linear system to get extremely accurate numerical solutions of circuit equations

SIMPLIS

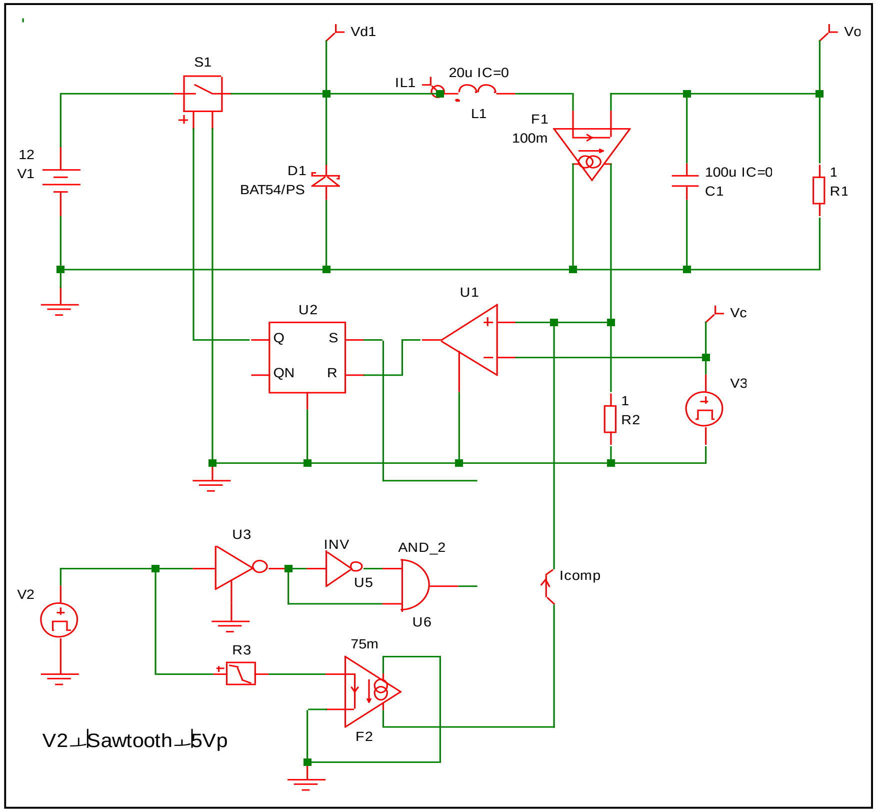
- **Because SIMPLIS can get extremely accurate numerical solutions to the circuit equations:**
  - **SIMPLIS can solve numerically for the steady-state limit cycle of a closed-loop switching power supply very quickly**
    - % change in all state variables from beginning to end of one conversion cycle < **10^{-10} %**
  - **SIMPLIS can perform a small signal analysis on the full large signal model of the power supply** (no need to derive a separate averaged model)

http://www.simplistechnologies.com/docs

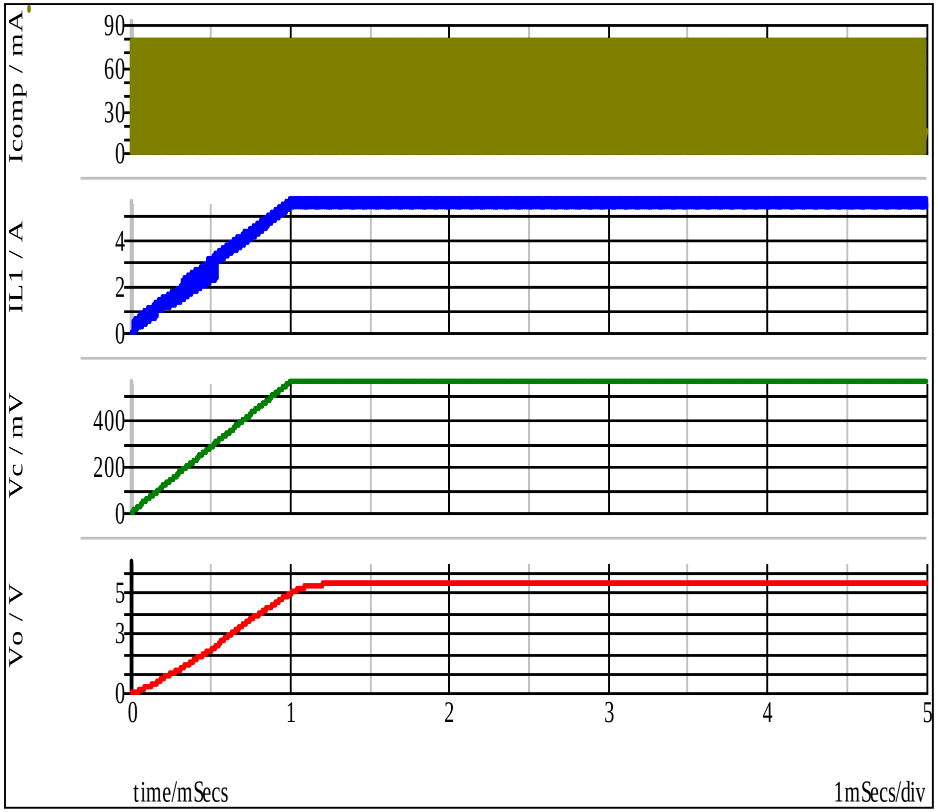
Contents

1. PE(Power Electronics) and Simulation
2. SIMetrix/SIMPLIS 특징
3. Components SPICE/PWL Model
4. PE Example
   - -Non Insulation type
     - -Buck type DC-DC Converter
     - -Boost type DC-DC Converter
     - -Boost type AC-DC Converter
   - -Insulation type
     - -Flyback DC-DC Converter
     - -Full Bridge DC-DC Converter
   - -Single Phase DC-AC Inverter

4-1. Buck DC/DC Converter Design Base on the SIMetrix/SIMPLIS Simulator

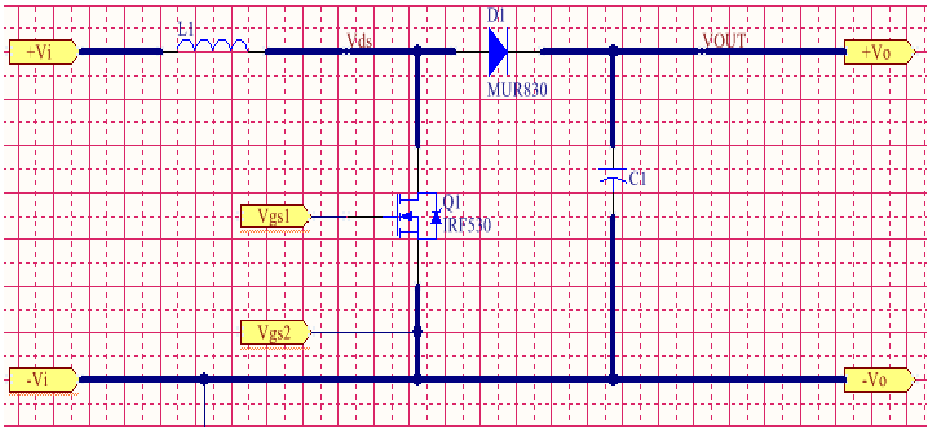


Current Mode Control
Buck DC-DC Converter

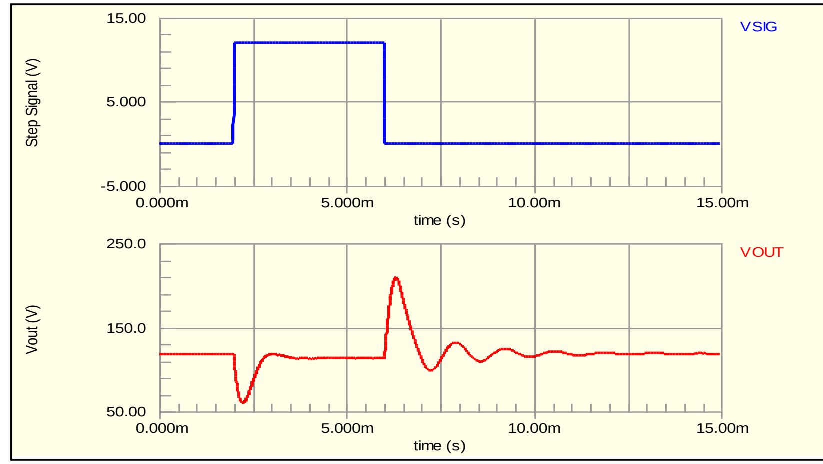


Start Response

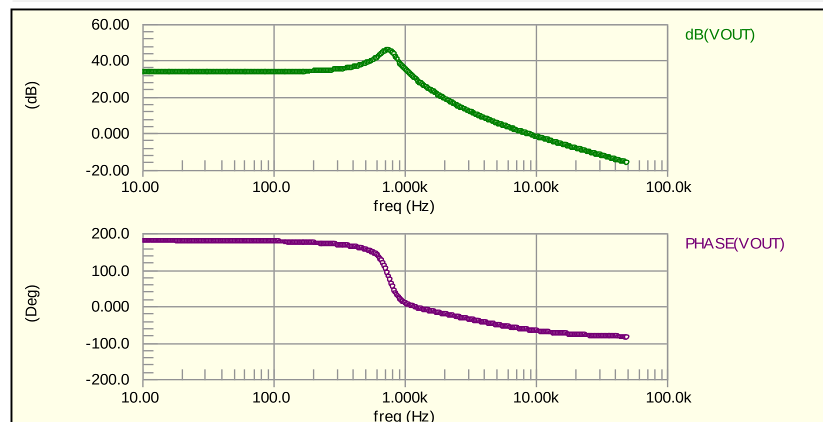
4-2 Base on the Altium Designer Using SIMPLIS Simulator



Boost DC-DC Converter Design Base on the Altium Schematic

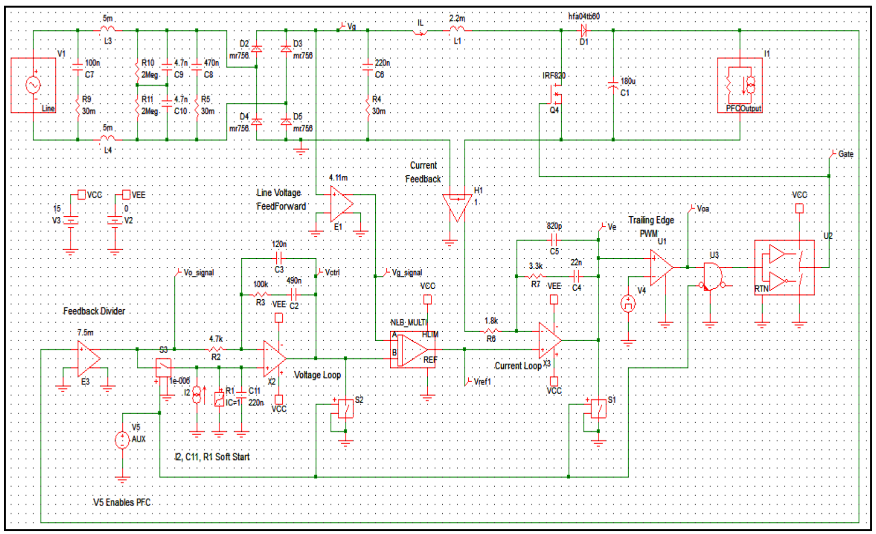


Step Response

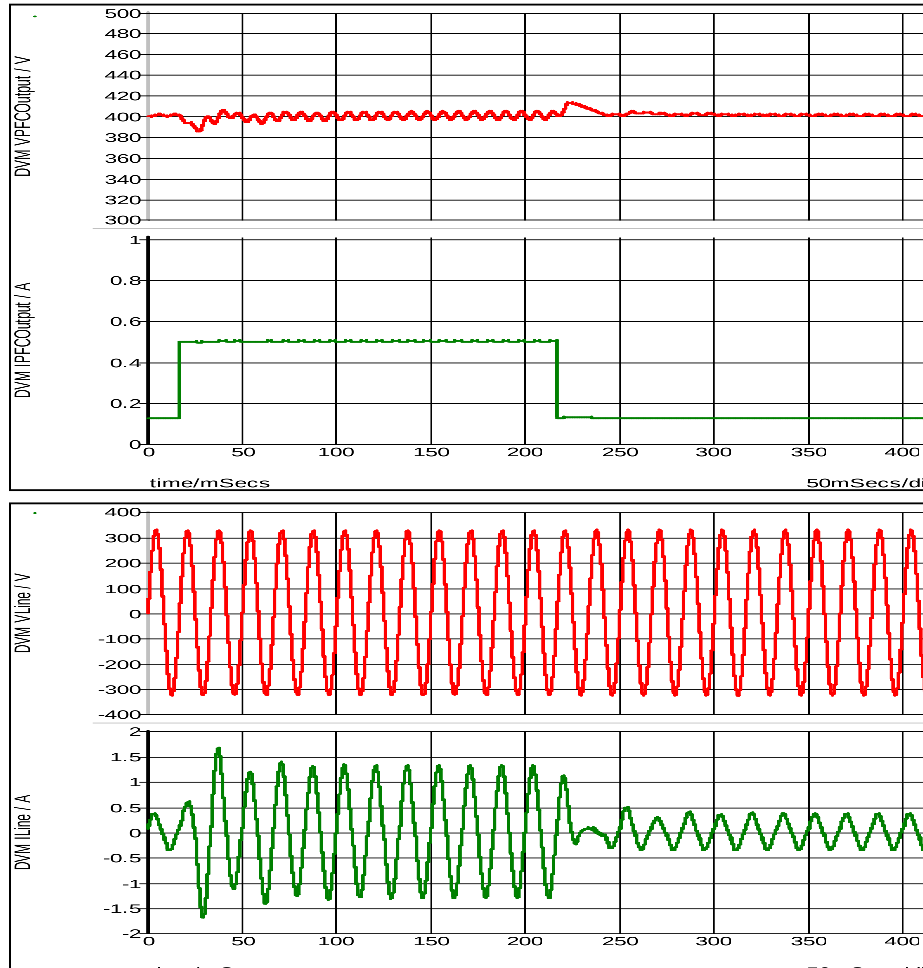


Frequency Response

4-3 Single Phase AC-DC Converter(SIMetrix) -Average Current Control Method

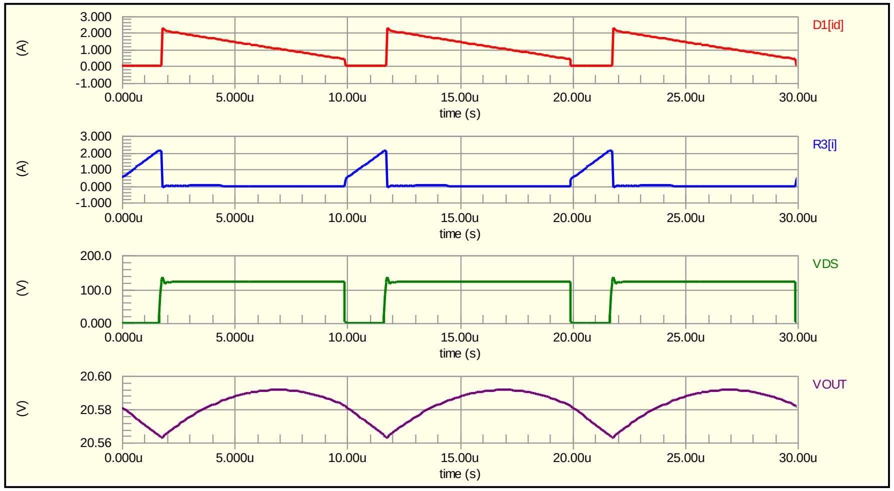


Single Phase AC-DC Converter

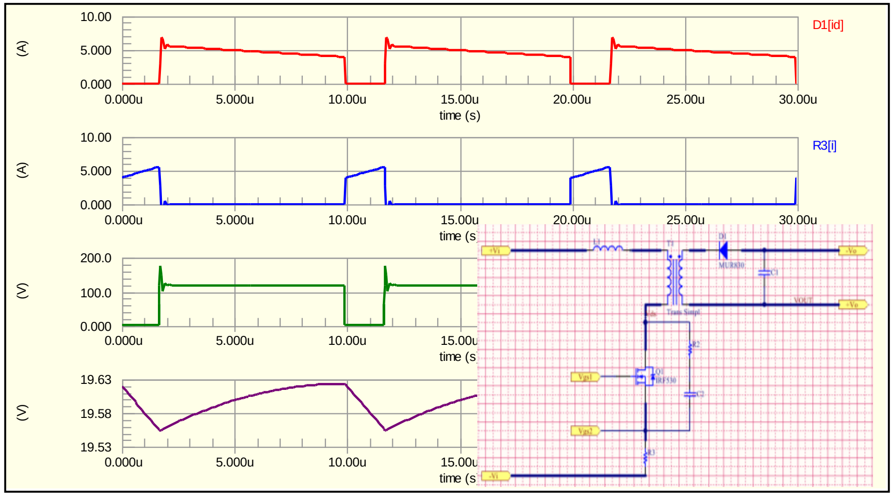


Load Step Response

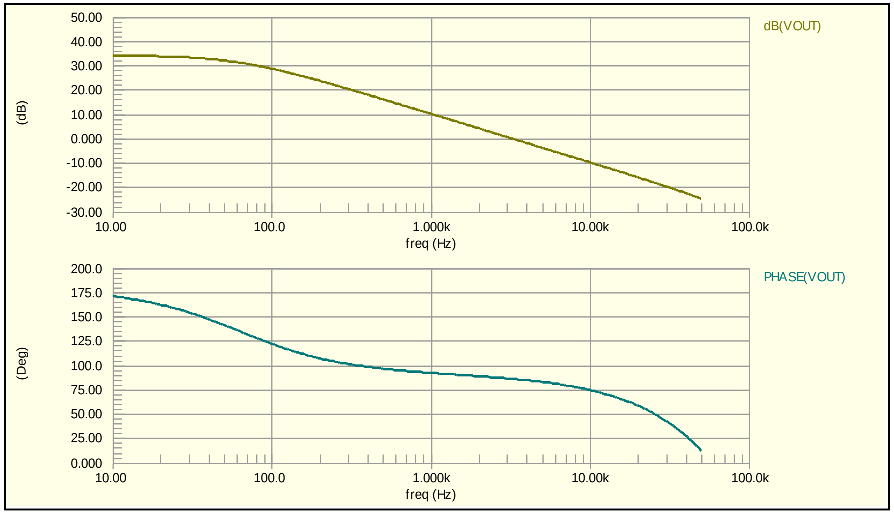
4-4 Flyback DC/DC Conv.
Design Base on the Altium Schematic



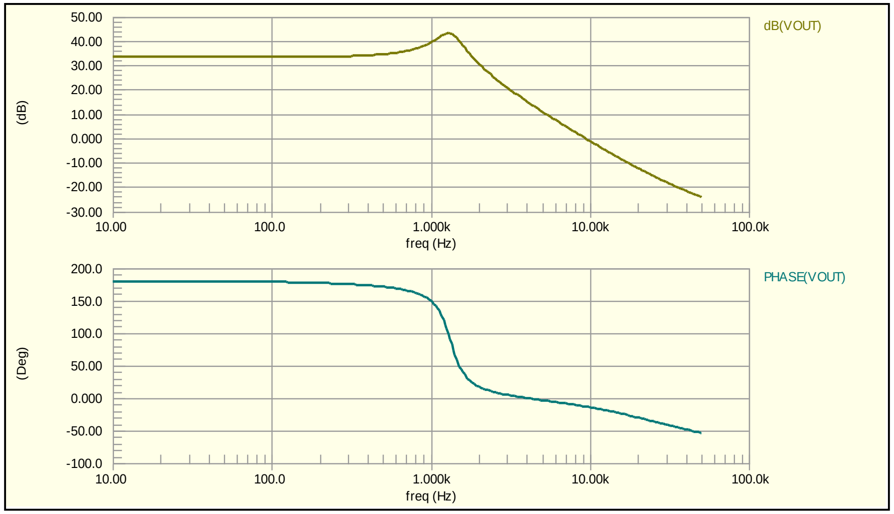
Switching Waveform (DCM)



Switching Waveform (CCM)

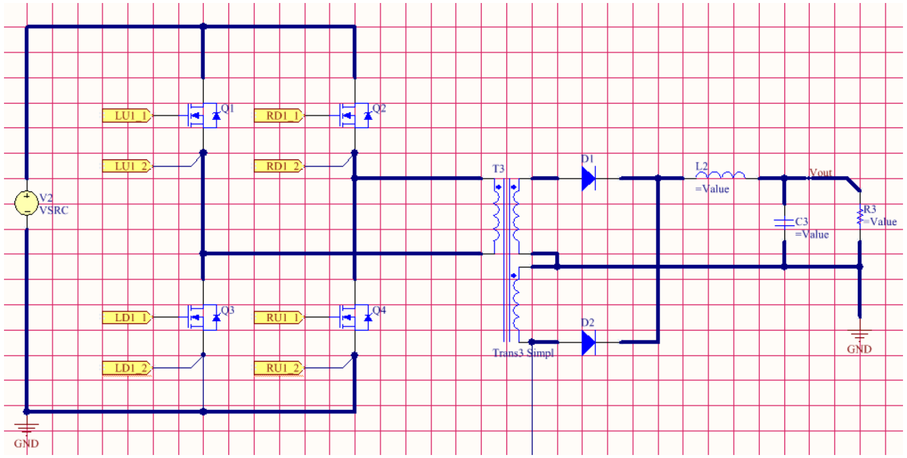


Frequency Response (DCM)

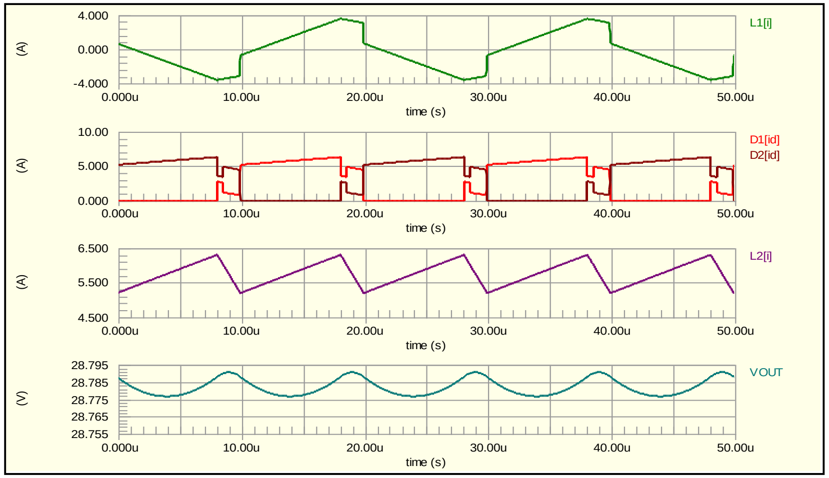


Frequency Response (CCM)

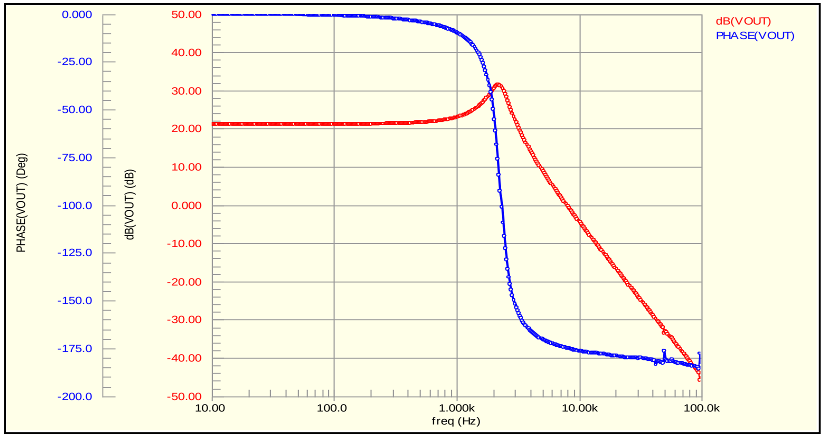
4-5.Base on the Altium Designer Using SIMPLIS Simulator(1/2)



Phase Shift Full Bridge
DC-DC Converter Design
Base on the Altium Schematic

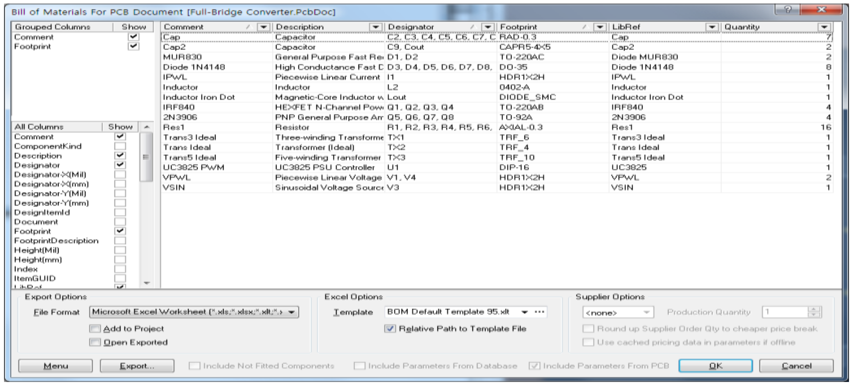


Switching Waveform

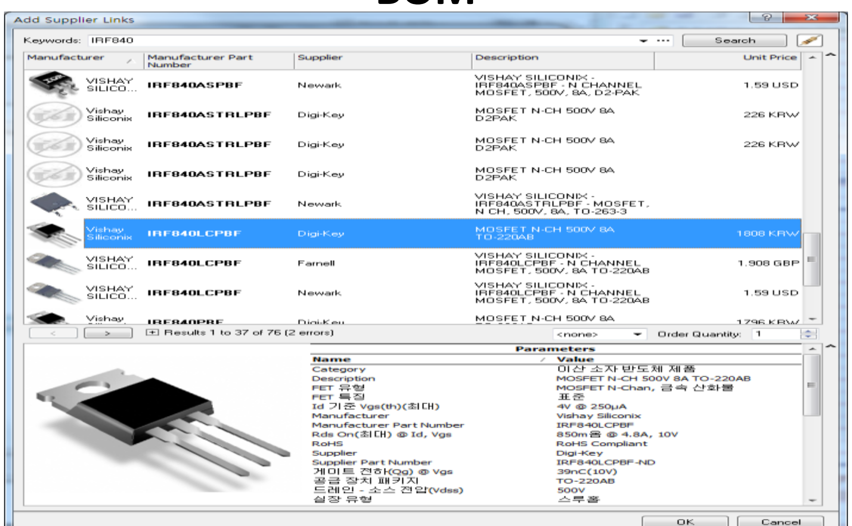


Frequency Response

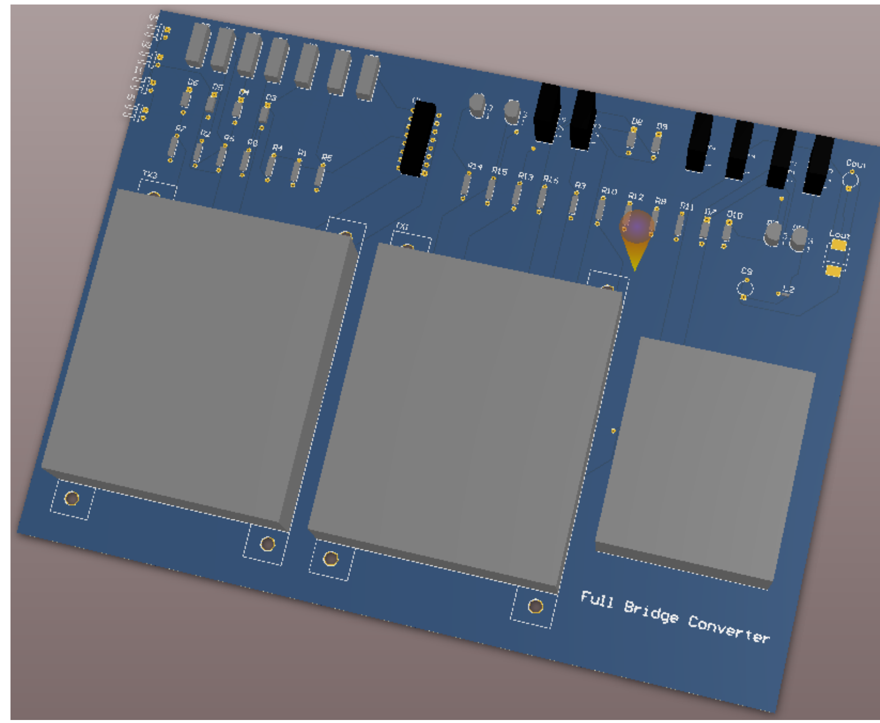
4-5. Base on the Altium Designer Using SIMPLIS Simulator (2/2)



BOM



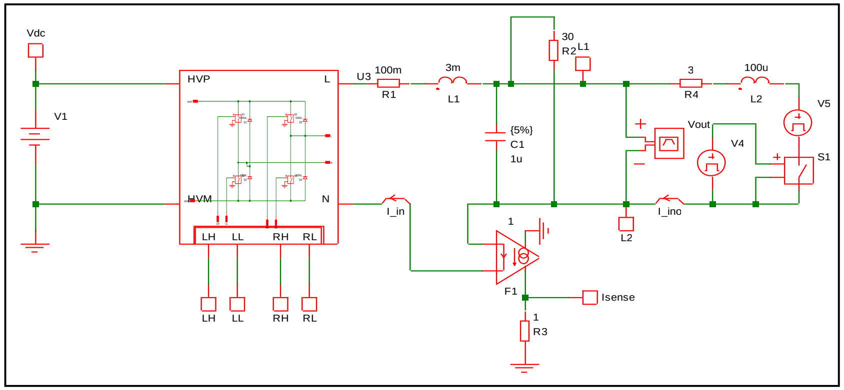
Supplier Link



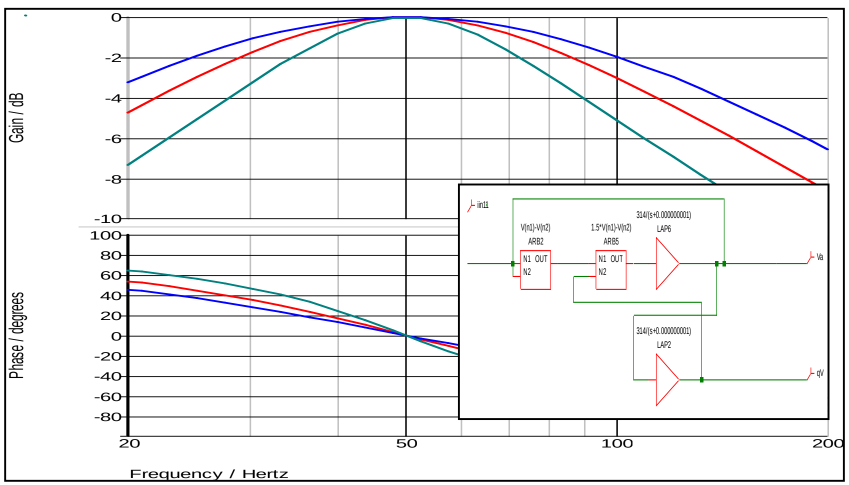
PCB

intergratech™

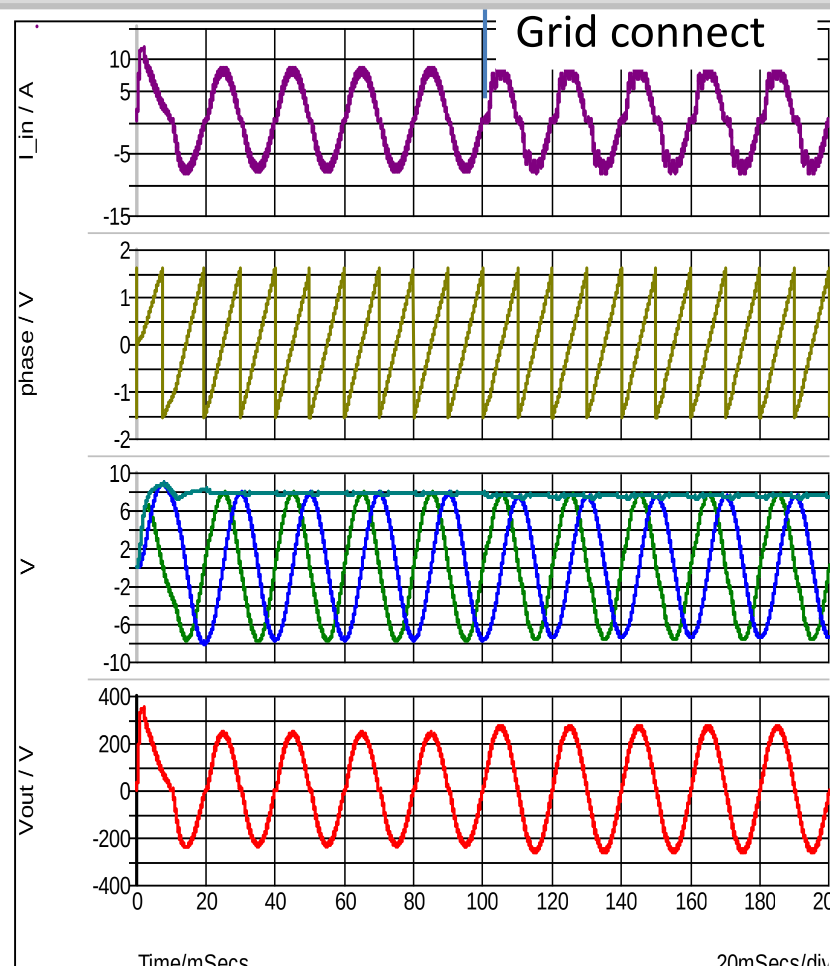
4-6. Development of Single Phase Inverter Using SOGI PLL Control Method



Inverter main circuit



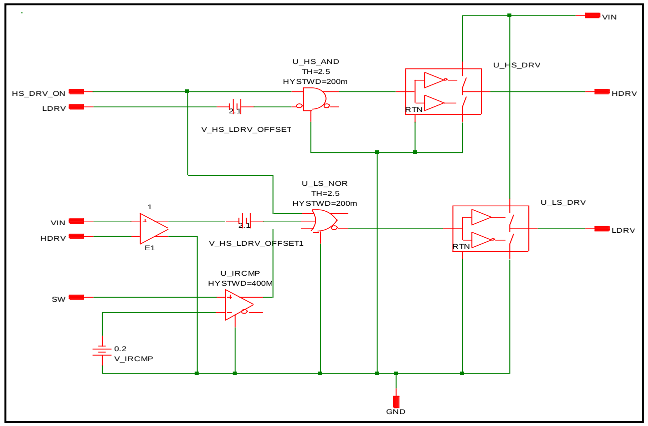
SOGI PLL Control



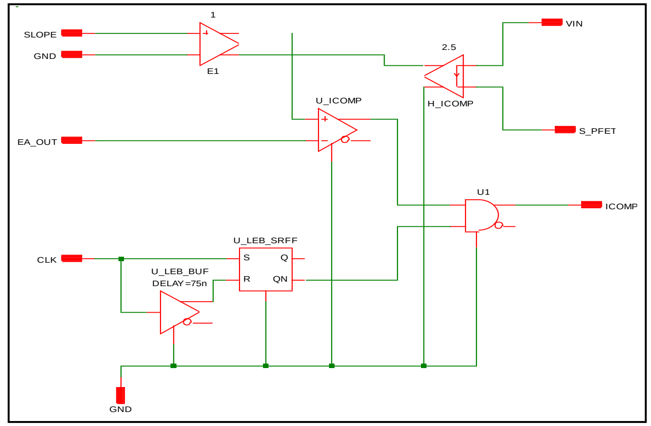
Waveform

intergratech™

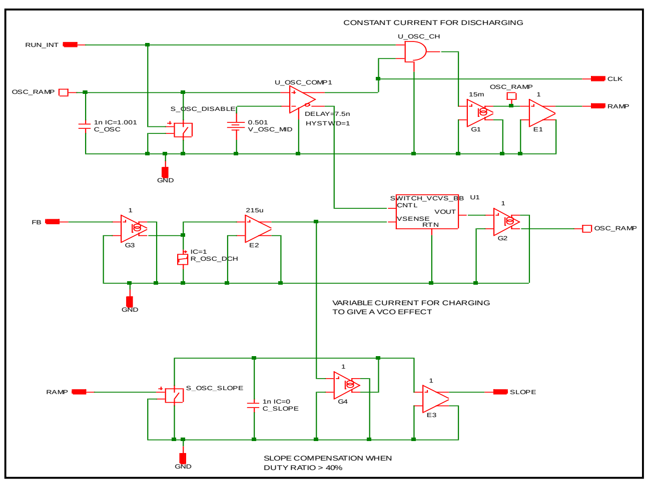
4-7. Control IC Design & Hierarchy Structure



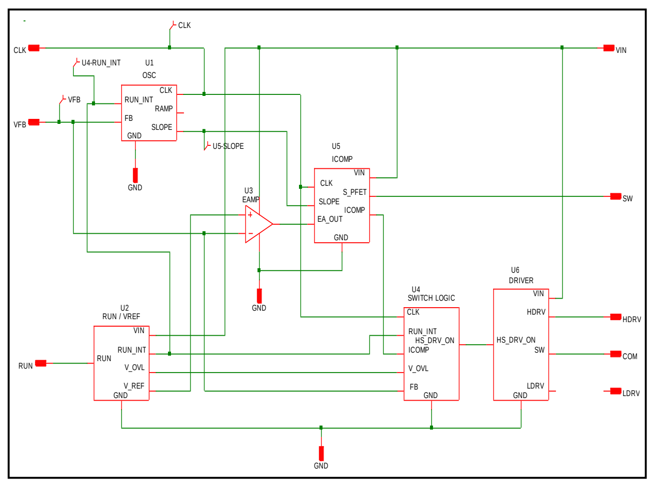
Drive Circuit



Switching Logic

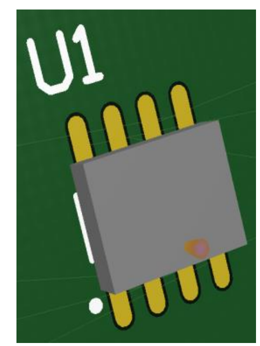


Function / Feedback Block



Control IC

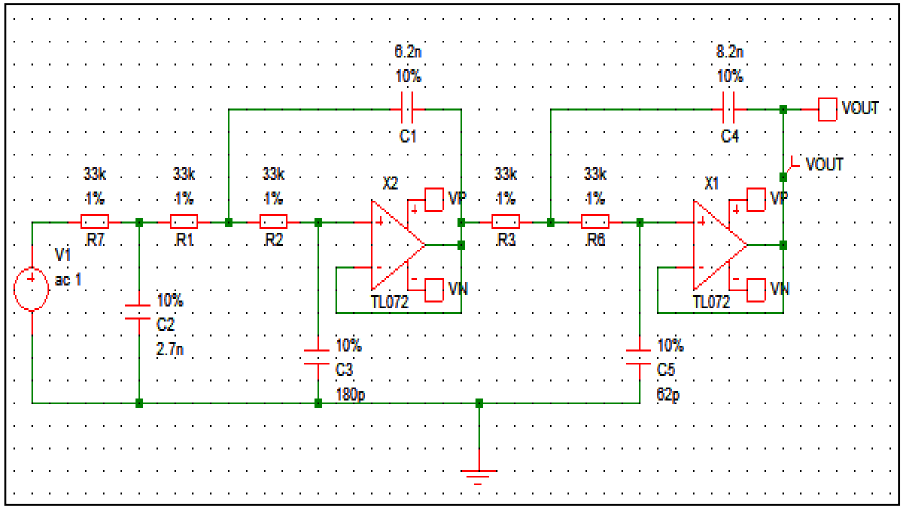
- Simulation Library
- Circuit Symbol
- Footprint
- PCB 3D



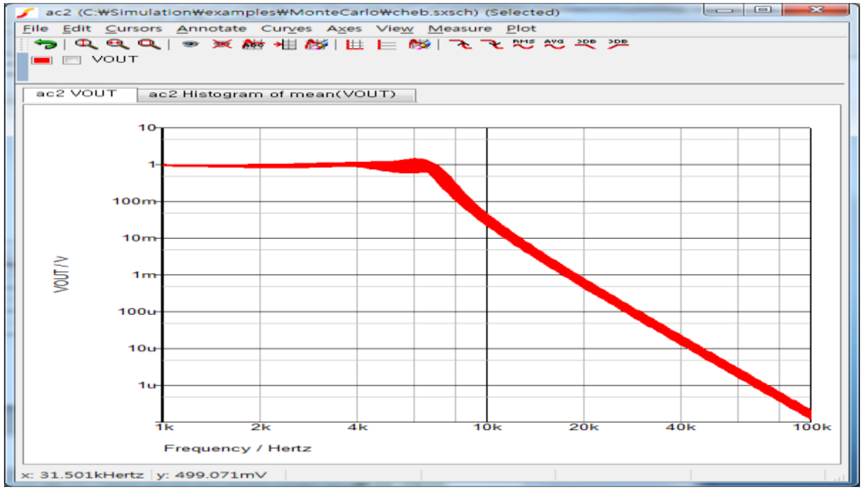
Footprint & PCB 3D

intergratech™

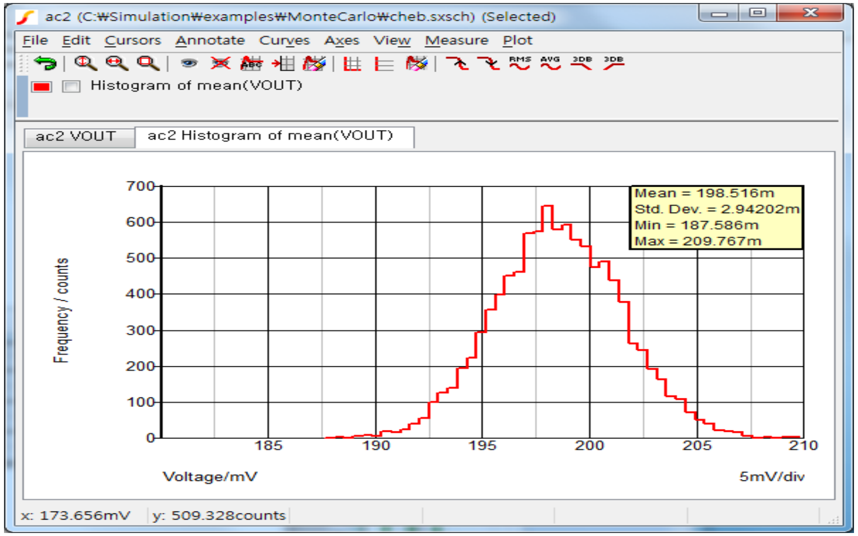
4-8. Monte-Carlo Analysis



Active filter



Response Result



Histogram

intergratech™

4-9. DVM(Design Verification Module)(1/2)

-AC Analysis

- **Bode Plot, Conducted Susceptibility, Input Impedance, Output Impedance**

-Transient Analysis

- **Step Load, Step Line, Startup, Short Circuit**

-DC-DC, AC-DC Steady-State Analysis

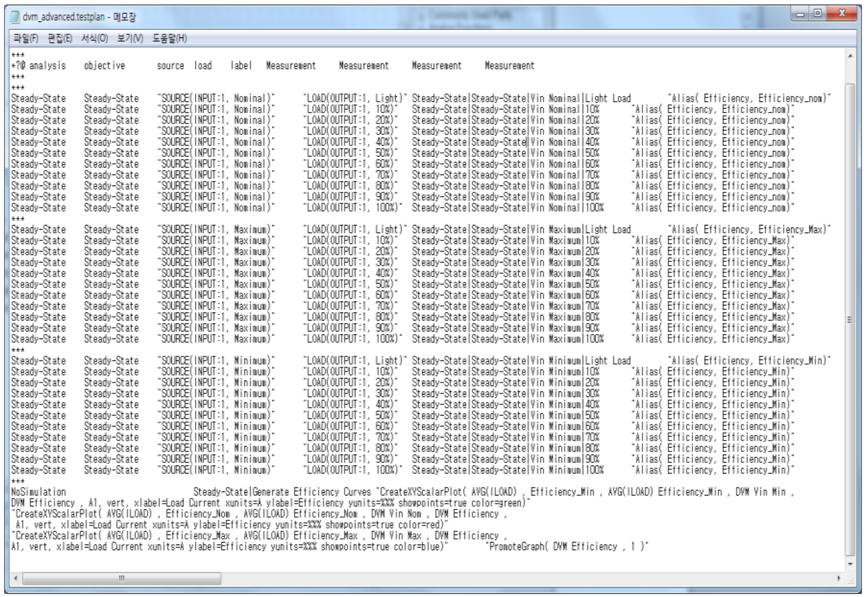
- **POP(Periodic Operating Point)(Only DC-DC),**
- **Line and Load Regulation, Efficiency, Power loss**
- **AC Analysis(Only DC-DC), Input/Output Impedance**

-Sensitivity / Worst Case Analysis

- **-Audit Circuit for Worst Case, Definition**

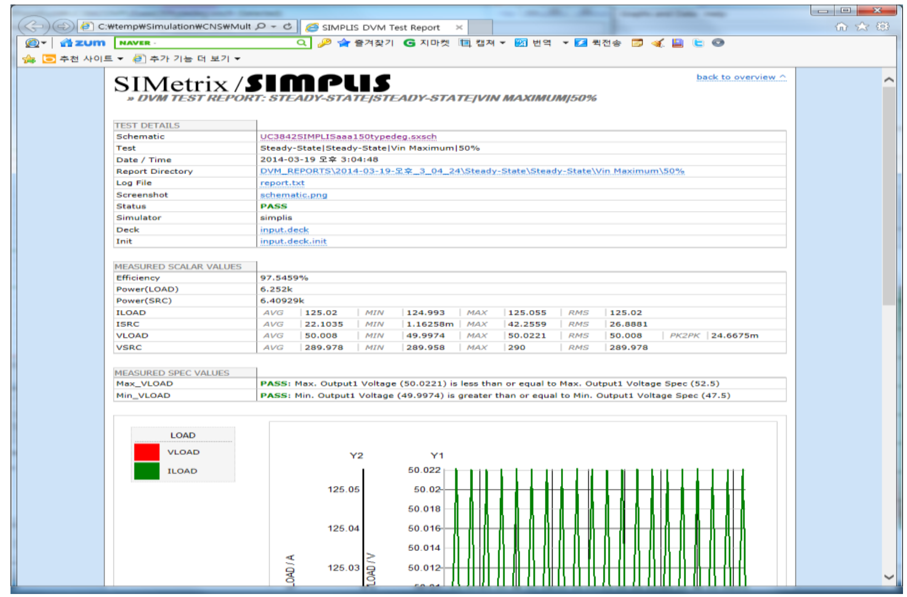
intergratech™

4-9. DVM(Design Verification Module)(2/2)



```
dvm_advanced.testplan - 메모장
파일(F) 편집(E) 서식(O) 보기(V) 도움말(H)
***
*?@ analysis	objective	source	load	label	Measurement	Measurement	Measurement	Measurement
***
***
Steady-State	Steady-State	"SOURCE(INPUT:1, Nominal)"	"LOAD(OUTPUT:1, Light)"	Steady-State|Steady-State|Vin Nominal|Light Load	"Alias( Efficiency, Efficiency_nom)"
Steady-State	Steady-State	"SOURCE(INPUT:1, Nominal)"	"LOAD(OUTPUT:1, 10%)"	Steady-State|Steady-State|Vin Nominal|10%	"Alias( Efficiency, Efficiency_nom)"
Steady-State	Steady-State	"SOURCE(INPUT:1, Nominal)"	"LOAD(OUTPUT:1, 20%)"	Steady-State|Steady-State|Vin Nominal|20%	"Alias( Efficiency, Efficiency_nom)"
Steady-State	Steady-State	"SOURCE(INPUT:1, Nominal)"	"LOAD(OUTPUT:1, 30%)"	Steady-State|Steady-State|Vin Nominal|30%	"Alias( Efficiency, Efficiency_nom)"
Steady-State	Steady-State	"SOURCE(INPUT:1, Nominal)"	"LOAD(OUTPUT:1, 40%)"	Steady-State|Steady-State|Vin Nominal|40%	"Alias( Efficiency, Efficiency_nom)"
Steady-State	Steady-State	"SOURCE(INPUT:1, Nominal)"	"LOAD(OUTPUT:1, 50%)"	Steady-State|Steady-State|Vin Nominal|50%	"Alias( Efficiency, Efficiency_nom)"
Steady-State	Steady-State	"SOURCE(INPUT:1, Nominal)"	"LOAD(OUTPUT:1, 60%)"	Steady-State|Steady-State|Vin Nominal|60%	"Alias( Efficiency, Efficiency_nom)"
Steady-State	Steady-State	"SOURCE(INPUT:1, Nominal)"	"LOAD(OUTPUT:1, 70%)"	Steady-State|Steady-State|Vin Nominal|70%	"Alias( Efficiency, Efficiency_nom)"
Steady-State	Steady-State	"SOURCE(INPUT:1, Nominal)"	"LOAD(OUTPUT:1, 80%)"	Steady-State|Steady-State|Vin Nominal|80%	"Alias( Efficiency, Efficiency_nom)"
Steady-State	Steady-State	"SOURCE(INPUT:1, Nominal)"	"LOAD(OUTPUT:1, 90%)"	Steady-State|Steady-State|Vin Nominal|90%	"Alias( Efficiency, Efficiency_nom)"
Steady-State	Steady-State	"SOURCE(INPUT:1, Nominal)"	"LOAD(OUTPUT:1, 100%)"	Steady-State|Steady-State|Vin Nominal|100%	"Alias( Efficiency, Efficiency_nom)"
***
Steady-State	Steady-State	"SOURCE(INPUT:1, Maximum)"	"LOAD(OUTPUT:1, Light)"	Steady-State|Steady-State|Vin Maximum|Light Load	"Alias( Efficiency, Efficiency_Max)"
Steady-State	Steady-State	"SOURCE(INPUT:1, Maximum)"	"LOAD(OUTPUT:1, 10%)"	Steady-State|Steady-State|Vin Maximum|10%	"Alias( Efficiency, Efficiency_Max)"
Steady-State	Steady-State	"SOURCE(INPUT:1, Maximum)"	"LOAD(OUTPUT:1, 20%)"	Steady-State|Steady-State|Vin Maximum|20%	"Alias( Efficiency, Efficiency_Max)"
Steady-State	Steady-State	"SOURCE(INPUT:1, Maximum)"	"LOAD(OUTPUT:1, 30%)"	Steady-State|Steady-State|Vin Maximum|30%	"Alias( Efficiency, Efficiency_Max)"
Steady-State	Steady-State	"SOURCE(INPUT:1, Maximum)"	"LOAD(OUTPUT:1, 40%)"	Steady-State|Steady-State|Vin Maximum|40%	"Alias( Efficiency, Efficiency_Max)"
Steady-State	Steady-State	"SOURCE(INPUT:1, Maximum)"	"LOAD(OUTPUT:1, 50%)"	Steady-State|Steady-State|Vin Maximum|50%	"Alias( Efficiency, Efficiency_Max)"
Steady-State	Steady-State	"SOURCE(INPUT:1, Maximum)"	"LOAD(OUTPUT:1, 60%)"	Steady-State|Steady-State|Vin Maximum|60%	"Alias( Efficiency, Efficiency_Max)"
Steady-State	Steady-State	"SOURCE(INPUT:1, Maximum)"	"LOAD(OUTPUT:1, 70%)"	Steady-State|Steady-State|Vin Maximum|70%	"Alias( Efficiency, Efficiency_Max)"
Steady-State	Steady-State	"SOURCE(INPUT:1, Maximum)"	"LOAD(OUTPUT:1, 80%)"	Steady-State|Steady-State|Vin Maximum|80%	"Alias( Efficiency, Efficiency_Max)"
Steady-State	Steady-State	"SOURCE(INPUT:1, Maximum)"	"LOAD(OUTPUT:1, 90%)"	Steady-State|Steady-State|Vin Maximum|90%	"Alias( Efficiency, Efficiency_Max)"
Steady-State	Steady-State	"SOURCE(INPUT:1, Maximum)"	"LOAD(OUTPUT:1, 100%)"	Steady-State|Steady-State|Vin Maximum|100%	"Alias( Efficiency, Efficiency_Max)"
***
Steady-State	Steady-State	"SOURCE(INPUT:1, Minimum)"	"LOAD(OUTPUT:1, Light)"	Steady-State|Steady-State|Vin Minimum|Light Load	"Alias( Efficiency, Efficiency_Min)"
Steady-State	Steady-State	"SOURCE(INPUT:1, Minimum)"	"LOAD(OUTPUT:1, 10%)"	Steady-State|Steady-State|Vin Minimum|10%	"Alias( Efficiency, Efficiency_Min)"
Steady-State	Steady-State	"SOURCE(INPUT:1, Minimum)"	"LOAD(OUTPUT:1, 20%)"	Steady-State|Steady-State|Vin Minimum|20%	"Alias( Efficiency, Efficiency_Min)"
Steady-State	Steady-State	"SOURCE(INPUT:1, Minimum)"	"LOAD(OUTPUT:1, 30%)"	Steady-State|Steady-State|Vin Minimum|30%	"Alias( Efficiency, Efficiency_Min)"
Steady-State	Steady-State	"SOURCE(INPUT:1, Minimum)"	"LOAD(OUTPUT:1, 40%)"	Steady-State|Steady-State|Vin Minimum|40%	"Alias( Efficiency, Efficiency_Min)"
Steady-State	Steady-State	"SOURCE(INPUT:1, Minimum)"	"LOAD(OUTPUT:1, 50%)"	Steady-State|Steady-State|Vin Minimum|50%	"Alias( Efficiency, Efficiency_Min)"
Steady-State	Steady-State	"SOURCE(INPUT:1, Minimum)"	"LOAD(OUTPUT:1, 60%)"	Steady-State|Steady-State|Vin Minimum|60%	"Alias( Efficiency, Efficiency_Min)"
Steady-State	Steady-State	"SOURCE(INPUT:1, Minimum)"	"LOAD(OUTPUT:1, 70%)"	Steady-State|Steady-State|Vin Minimum|70%	"Alias( Efficiency, Efficiency_Min)"
Steady-State	Steady-State	"SOURCE(INPUT:1, Minimum)"	"LOAD(OUTPUT:1, 80%)"	Steady-State|Steady-State|Vin Minimum|80%	"Alias( Efficiency, Efficiency_Min)"
Steady-State	Steady-State	"SOURCE(INPUT:1, Minimum)"	"LOAD(OUTPUT:1, 90%)"	Steady-State|Steady-State|Vin Minimum|90%	"Alias( Efficiency, Efficiency_Min)"
Steady-State	Steady-State	"SOURCE(INPUT:1, Minimum)"	"LOAD(OUTPUT:1, 100%)"	Steady-State|Steady-State|Vin Minimum|100%	"Alias( Efficiency, Efficiency_Min)"
***
NoSimulation		Steady-State|Generate Efficiency Curves "CreateXYScalarPlot( AVG(ILOAD) , Efficiency_Min , AVG(ILOAD) Efficiency_Min , DVM Vin Min ,
DVM Efficiency , A1, vert, xlabel=Load Current xunits=A ylabel=Efficiency yunits=%%% showpoints=true color=green)"
"CreateXYScalarPlot( AVG(ILOAD) , Efficiency_Nom , AVG(ILOAD) Efficiency_Nom , DVM Vin Nom , DVM Efficiency ,
 A1, vert, xlabel=Load Current xunits=A ylabel=Efficiency yunits=%%% showpoints=true color=red)"
"CreateXYScalarPlot( AVG(ILOAD) , Efficiency_Max , AVG(ILOAD) Efficiency_Max , DVM Vin Max , DVM Efficiency ,
A1, vert, xlabel=Load Current xunits=A ylabel=Efficiency yunits=%%% showpoints=true color=blue)"	"PromoteGraph( DVM Efficiency , 1 )"
```

DC/DC Converter Efficiency Test Plan



SIMPLIS DVM Test Report

SIMetrix / SIMPLIS

back to overview ^

» DVM TEST REPORT: STEADY-STATE|STEADY-STATE|VIN MAXIMUM|50%

TEST DETAILS	
Schematic	UC3842SIMPLISaaa150typedeg.sxsch
Test	Steady-State|Steady-State|Vin Maximum|50%
Date / Time	2014-03-19 오후 3:04:48
Report Directory	DVM_REPORTS\2014-03-19-오후_3_04_24\Steady-State\Steady-State\Vin Maximum\50%
Log File	report.txt
Screenshot	schematic.png
Status	PASS
Simulator	simplis
Deck	input.deck
Init	input.deck.init

MEASURED SCALAR VALUES										
Efficiency	97.5459%									
Power(LOAD)	6.252k									
Power(SRC)	6.40929k									
ILOAD	AVG	125.02	MIN	124.993	MAX	125.055	RMS	125.02		
ISRC	AVG	22.1035	MIN	1.16258m	MAX	42.2559	RMS	26.8881		
VLOAD	AVG	50.008	MIN	49.9974	MAX	50.0221	RMS	50.008	PK2PK	24.6675m
VSRC	AVG	289.978	MIN	289.958	MAX	290	RMS	289.978		

MEASURED SPEC VALUES	
Max_VLOAD	PASS: Max. Output1 Voltage (50.0221) is less than or equal to Max. Output1 Voltage Spec (52.5)
Min_VLOAD	PASS: Min. Output1 Voltage (49.9974) is greater than or equal to Min. Output1 Voltage Spec (47.5)

Test Report