SIMPLIS/SIMetrix
전원 CM 노이즈 평가 응용

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Contents

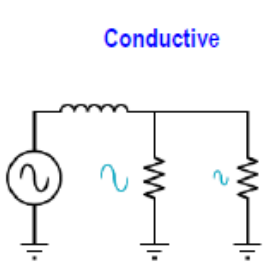
- **About Common mode noise..**
  . What's the C.M noise among many coupling routes
  . Why we need to consider C.M noise

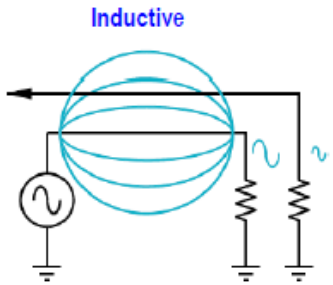
- **Power System level analysis**
  . Which factor can effect on C.M noise issue (parasitic L, C, etc..)
  . Obtain clear signal measurement by changing C.M current return path
  . Common mode Voltage ripple & noise Current decrease by changing Y-cap

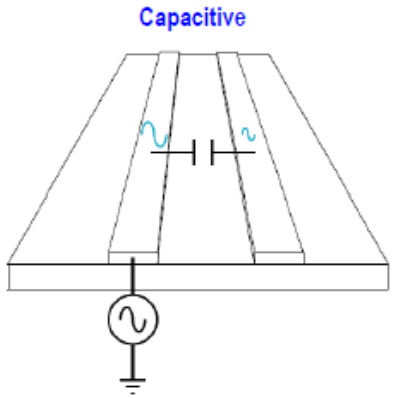
- **Simulation for C.M noise**
  . Circuits side
  . Minimize the power GND return current path
  . Minimize the C.M current return path

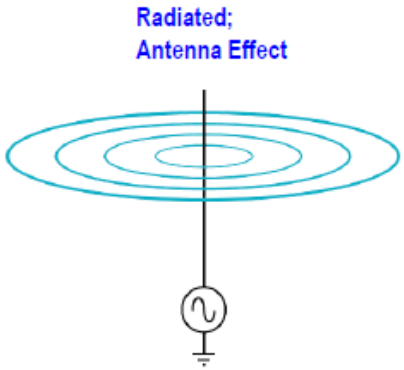
[EMI] Noise coupling route

- 4 standard kinds of noise coupling

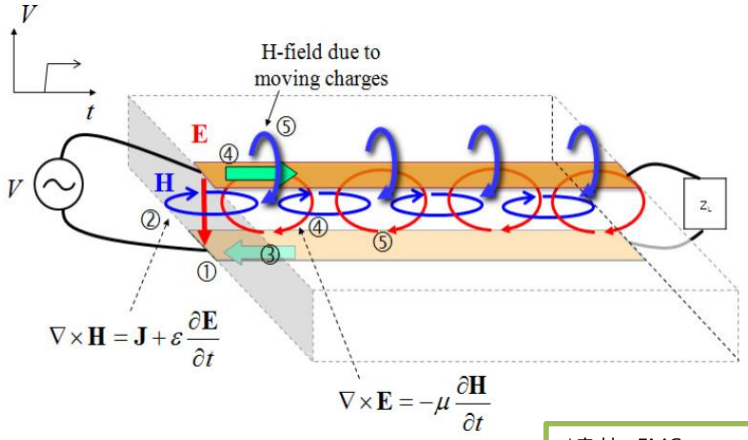






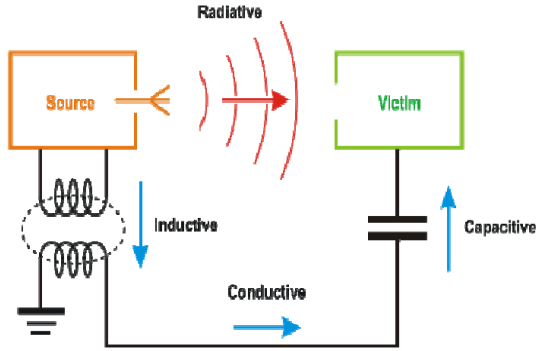


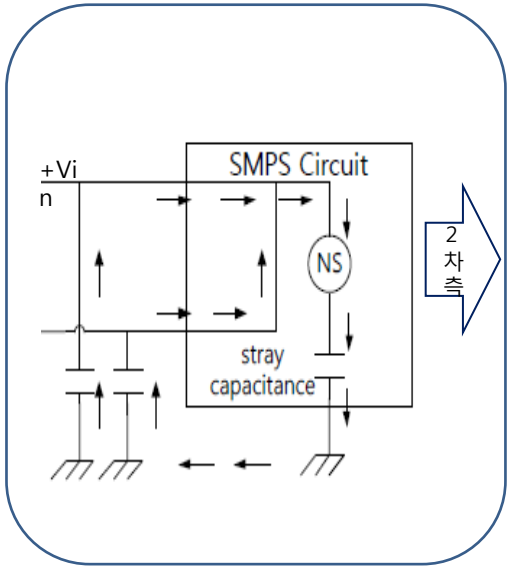
PCB E-field, H-field



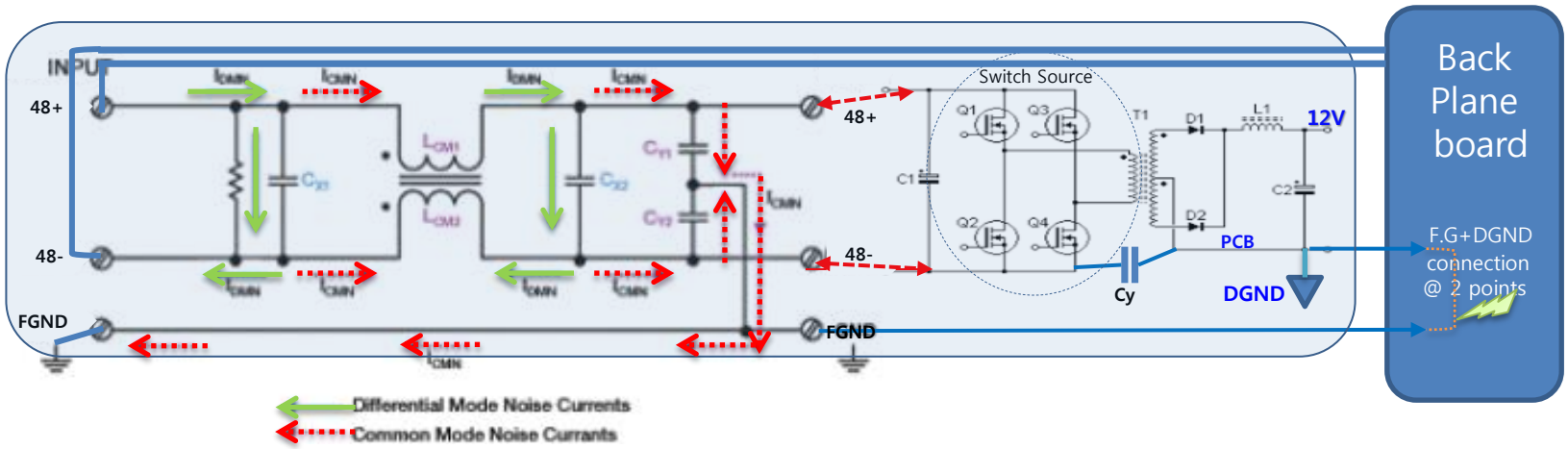
*출처 : EMC papers

Noise Coupling in PDN

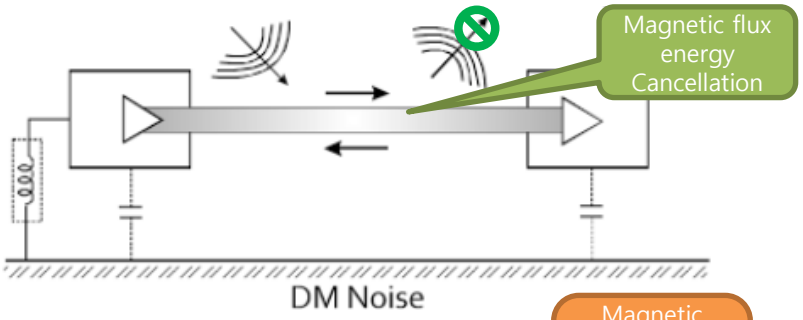


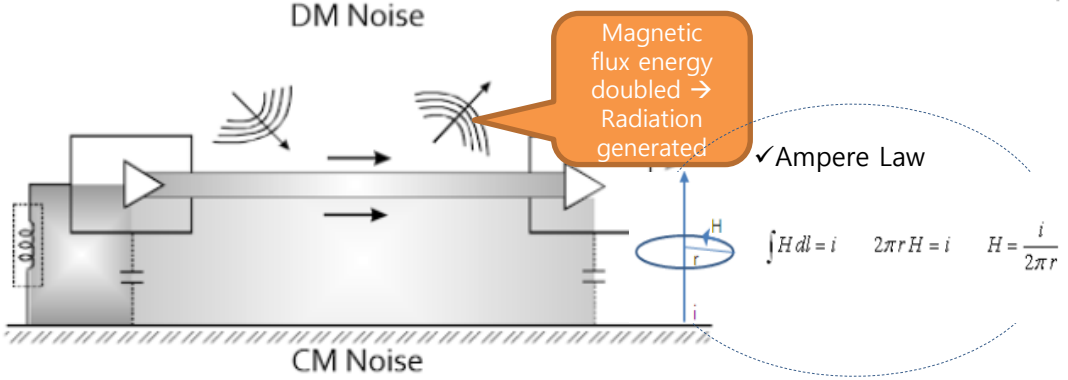


• What is Common mode noise?

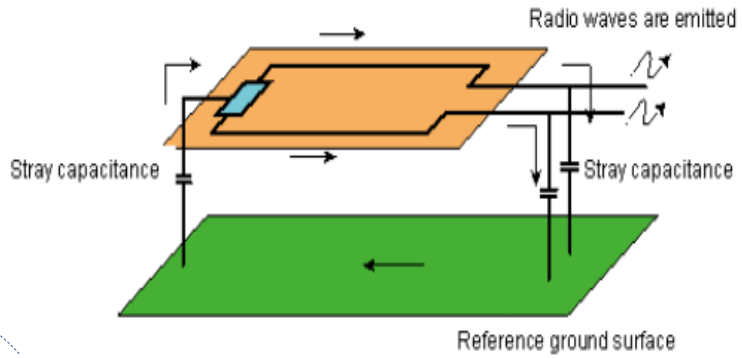


*Radiation to cable





*PCB Capacitive coupling

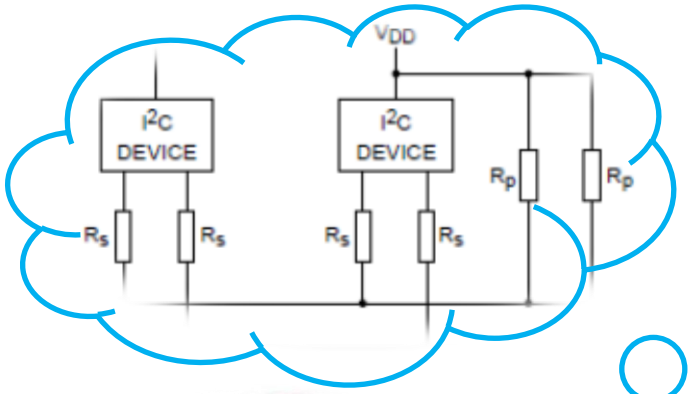


PCB GND Layer

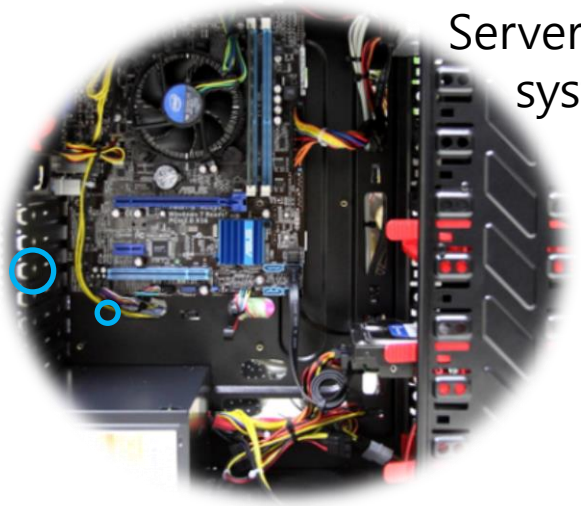
*출처 : EMC papers

Digital weakly specified I2C signal
vs.
Noisy Power line cable

I²C



Signal &
Power cable



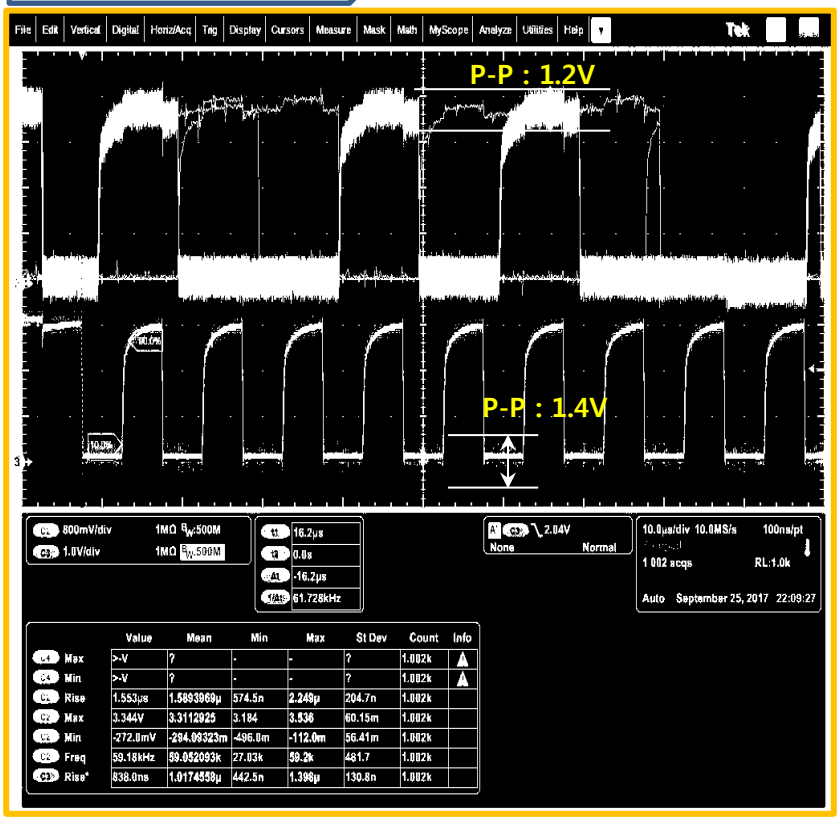
Server or PC
system

- **I2C line voltage noise under interfering with Power lines**

  . Noises are Synch. to the switching frequency of Power

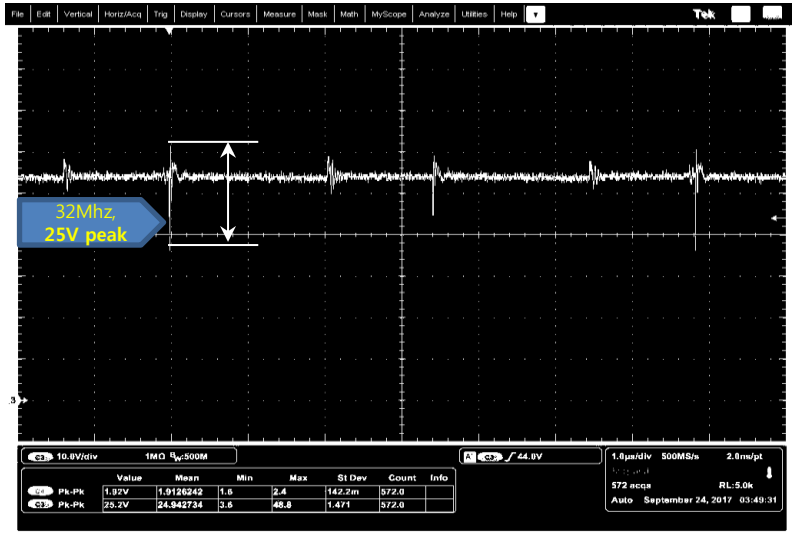
Faster Switch or some coupling line

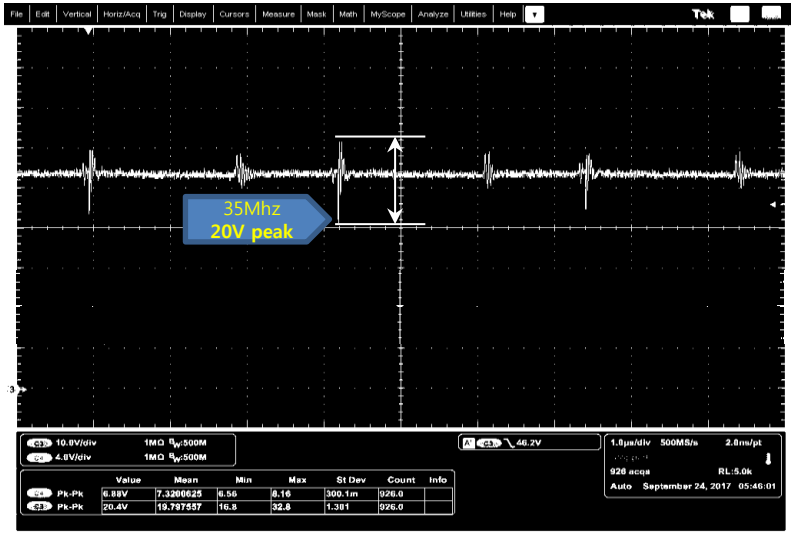
Slow Switch



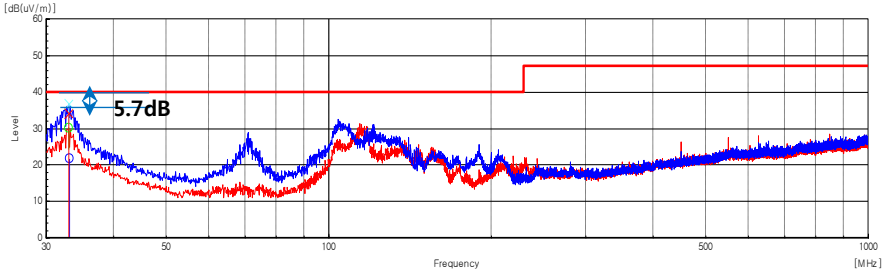
- **RE EMI source → Differential and Common mode noise (Primary +Vin ~ GND)**

  . FET Vds ringing noise level : **25V(Fast Switch) > 20V(Slow Switch) : 5[dB] scale margin**

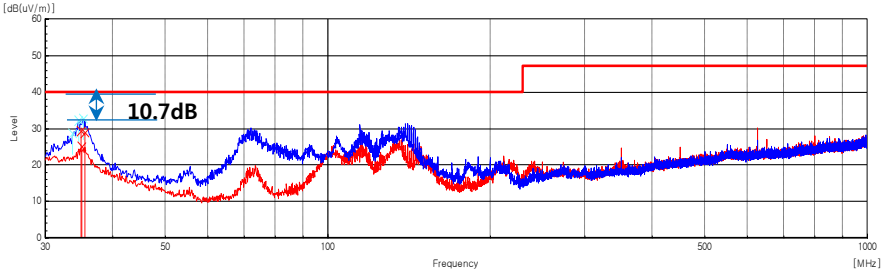




Fast Switch

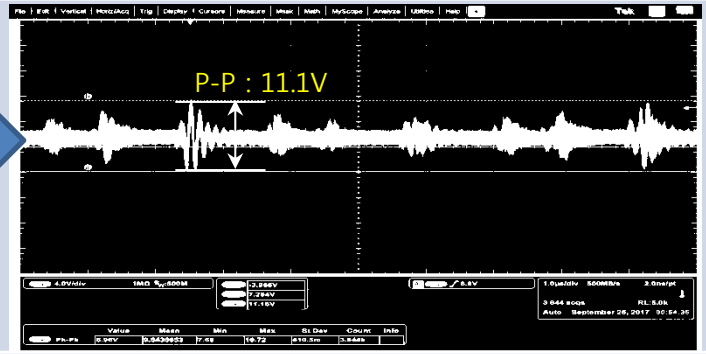
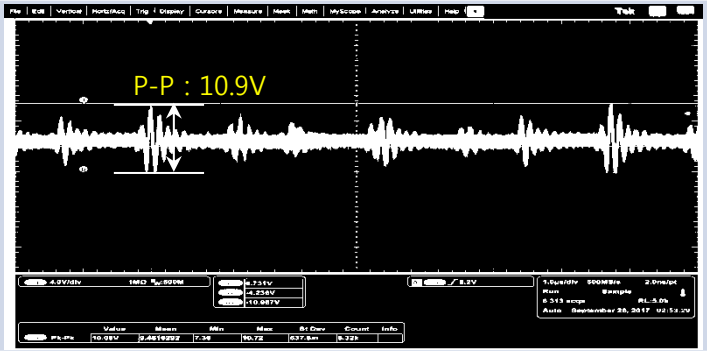
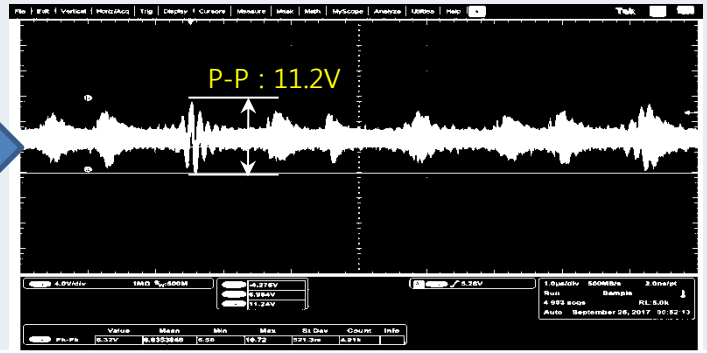
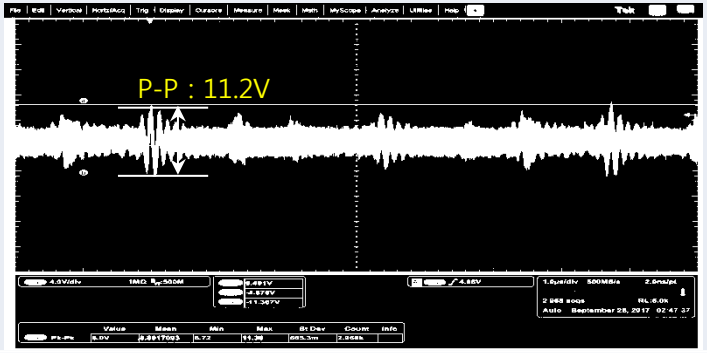
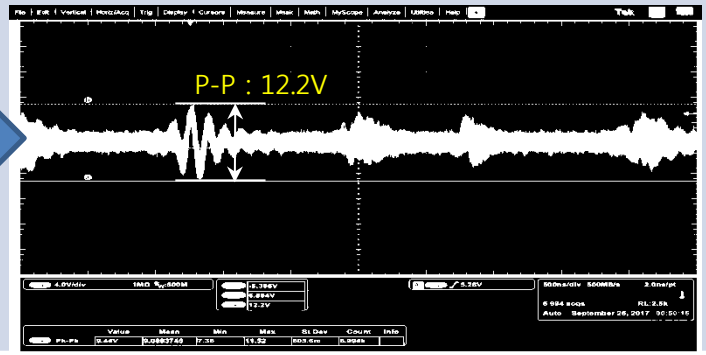
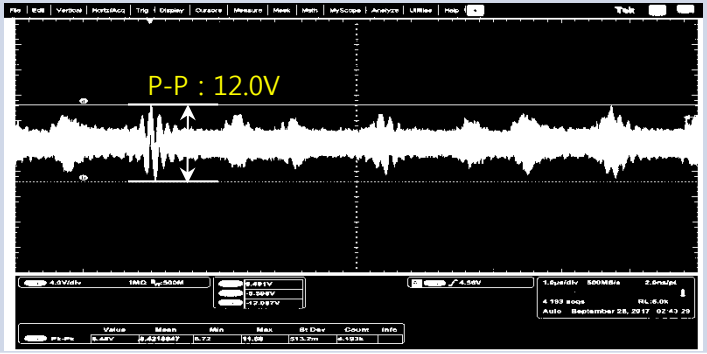


Slow Switch



. RE noise

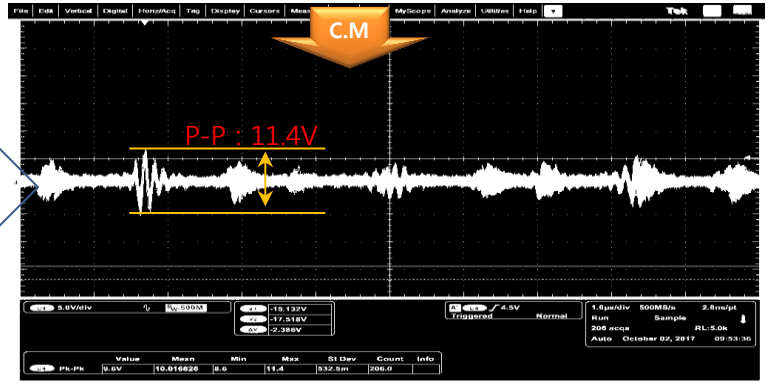
- Single b'd : only → 6.7V peak to peak(same /w simulation) vs. Multi b'd

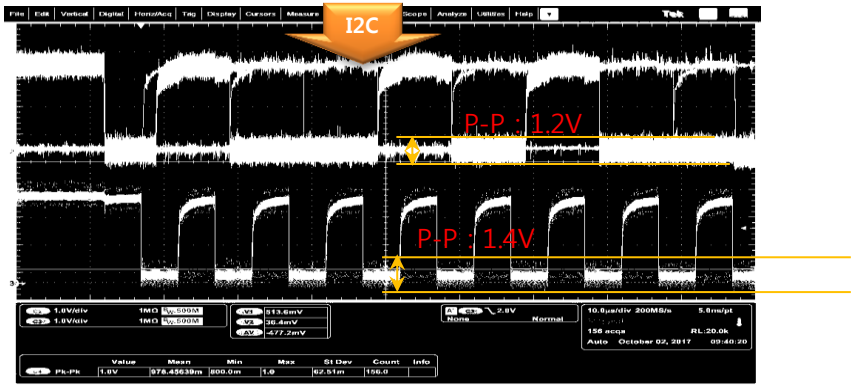
	High Speed Switch	Low Speed Switch
1+1 b'ds		
1+2 b'ds		
1+3 b'ds		

B'd 'A', B'd 'B' : Y-cap line 보드내 연결 전/후

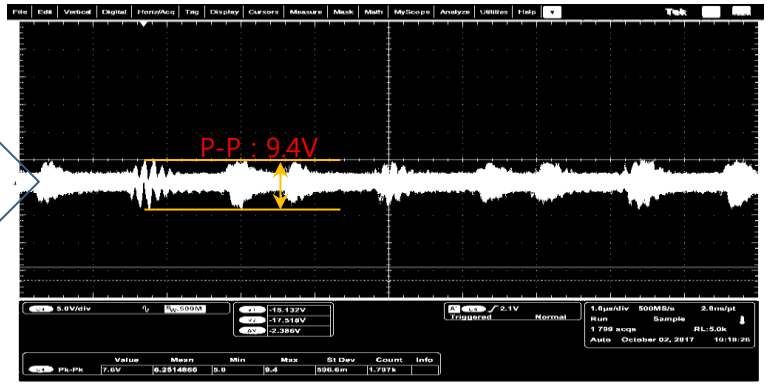
※ B'd 'B'에 FET Rising Switching이 빠른 것**(Typ. 4nS)** 으로 적용 후 측정 data

Origin

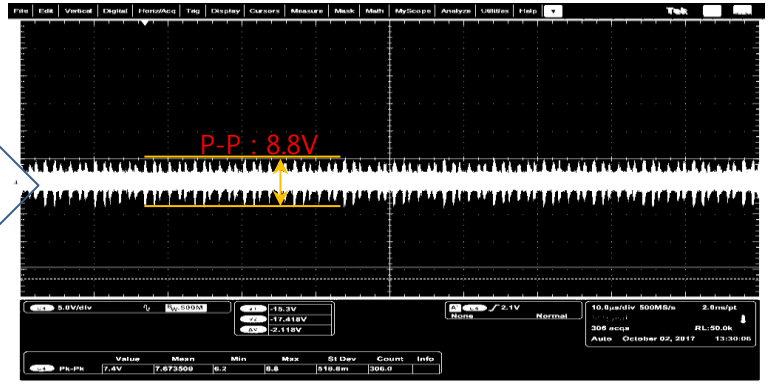


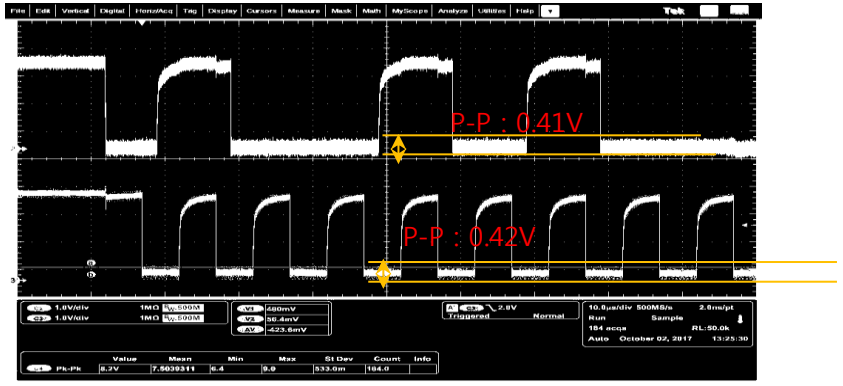


Only B'd 'A' Y-cap line 강화



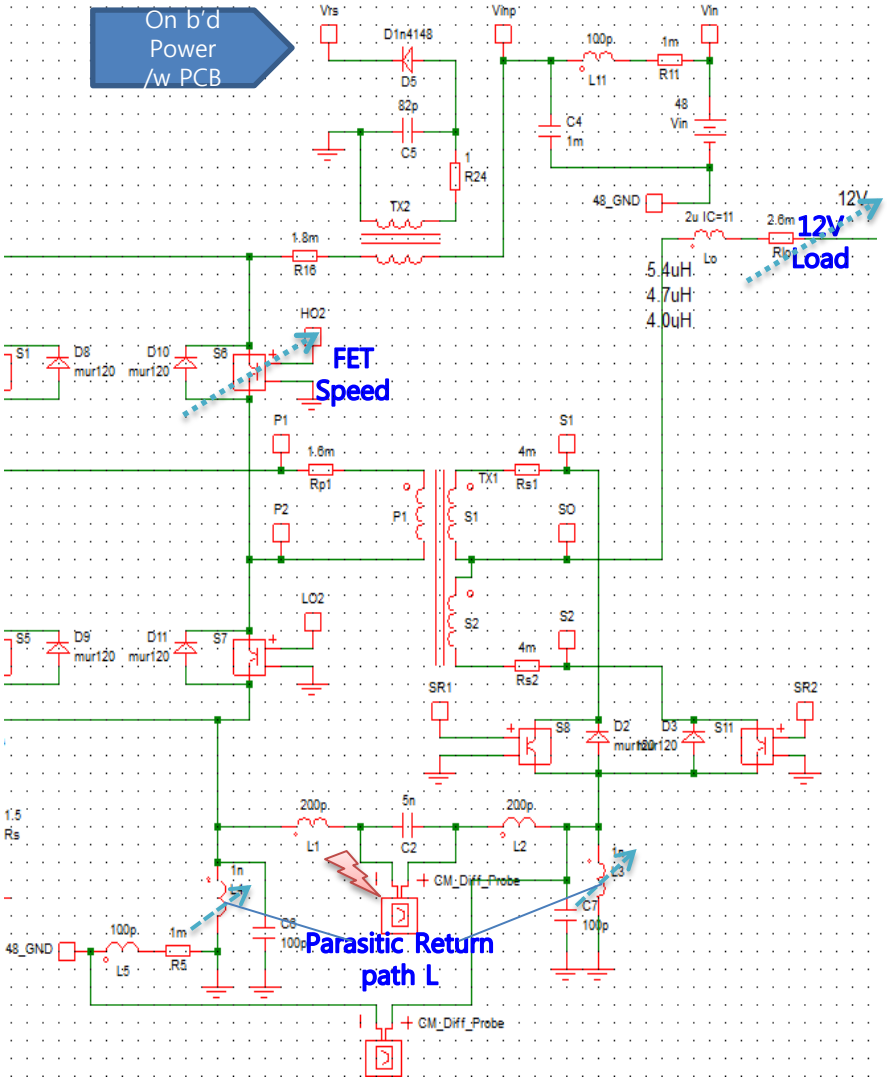
B'd 'A', B'd 'B' Y-Cap line 강화

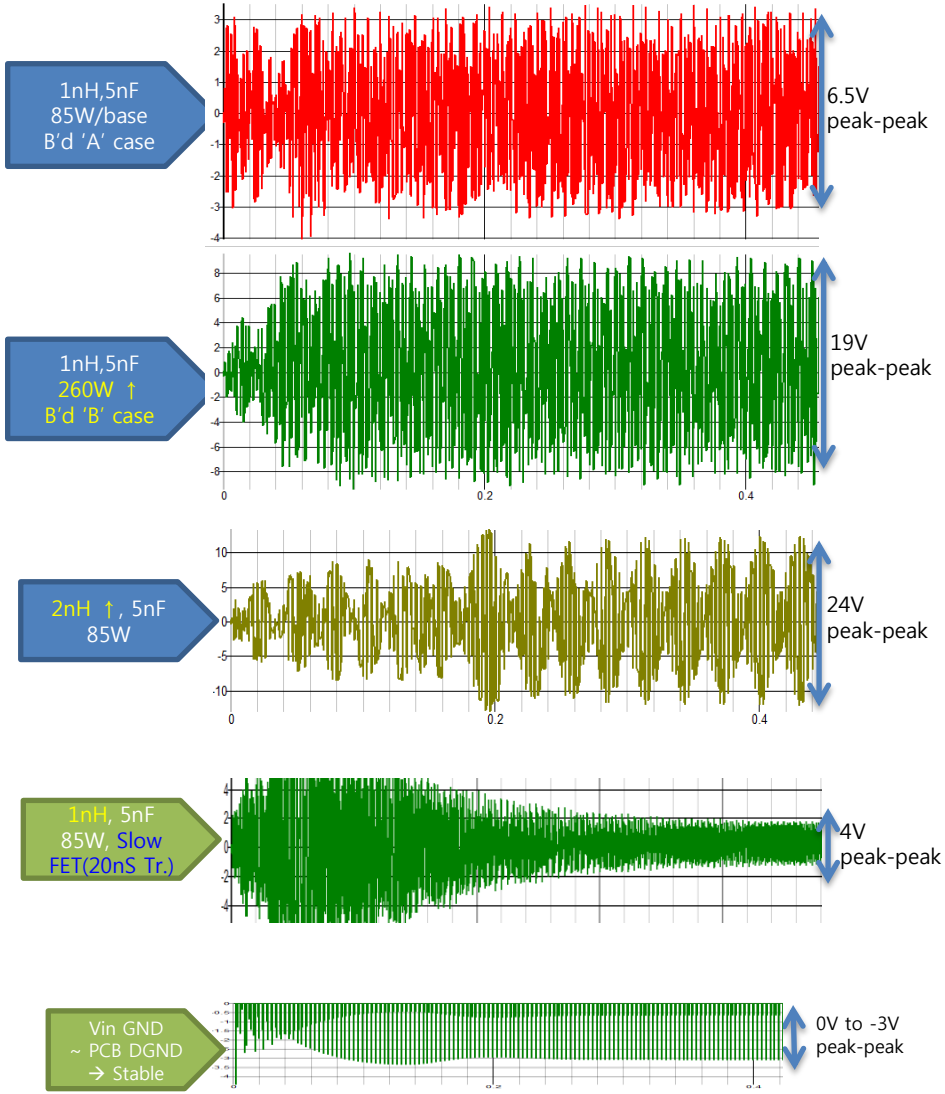




CM Ground voltage Gap (Relative CM leakage value)

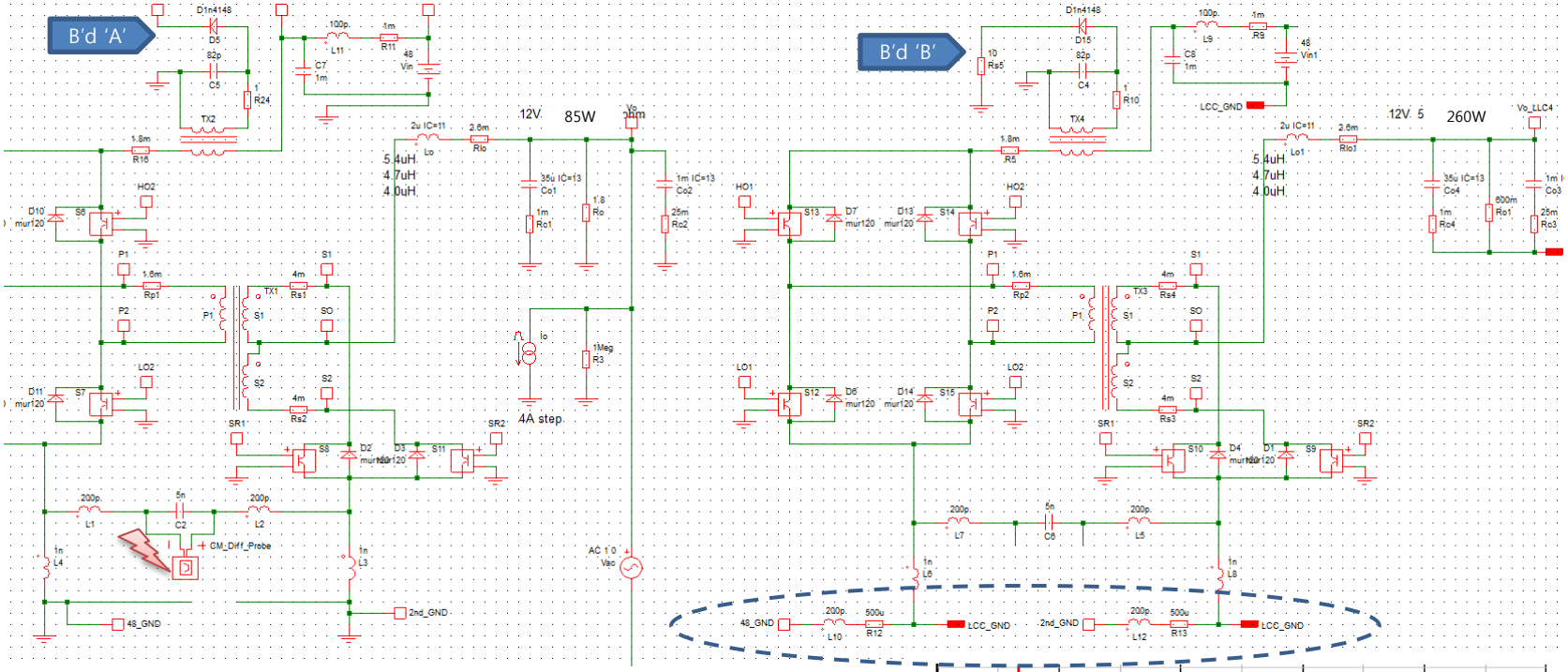
- Load & PCB return-L effect

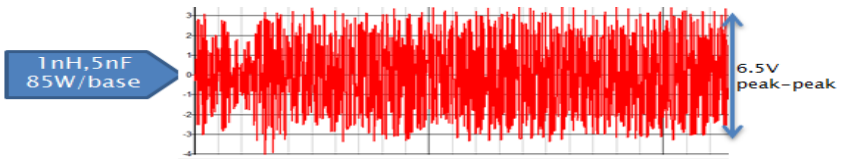


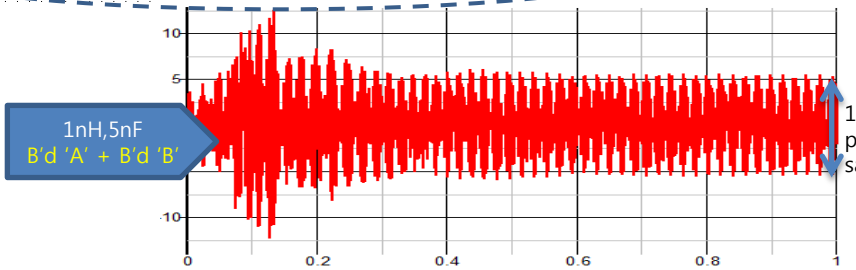


CM 1st~2nd Ground voltage gap Simulation

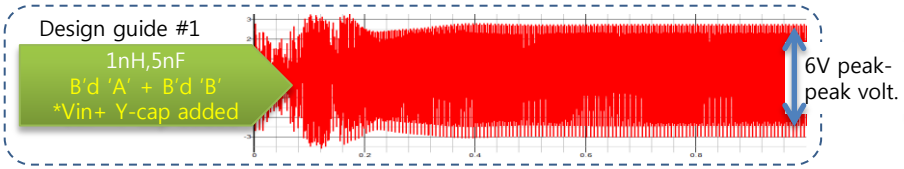
- Add B'd 'B' x1pcs on the back

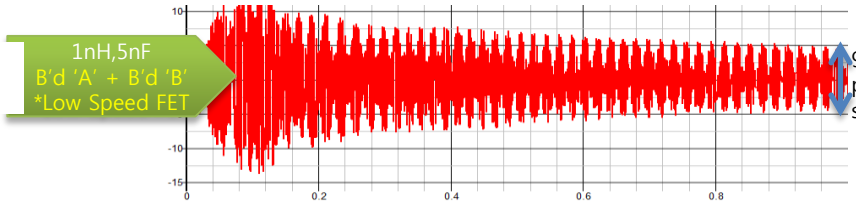






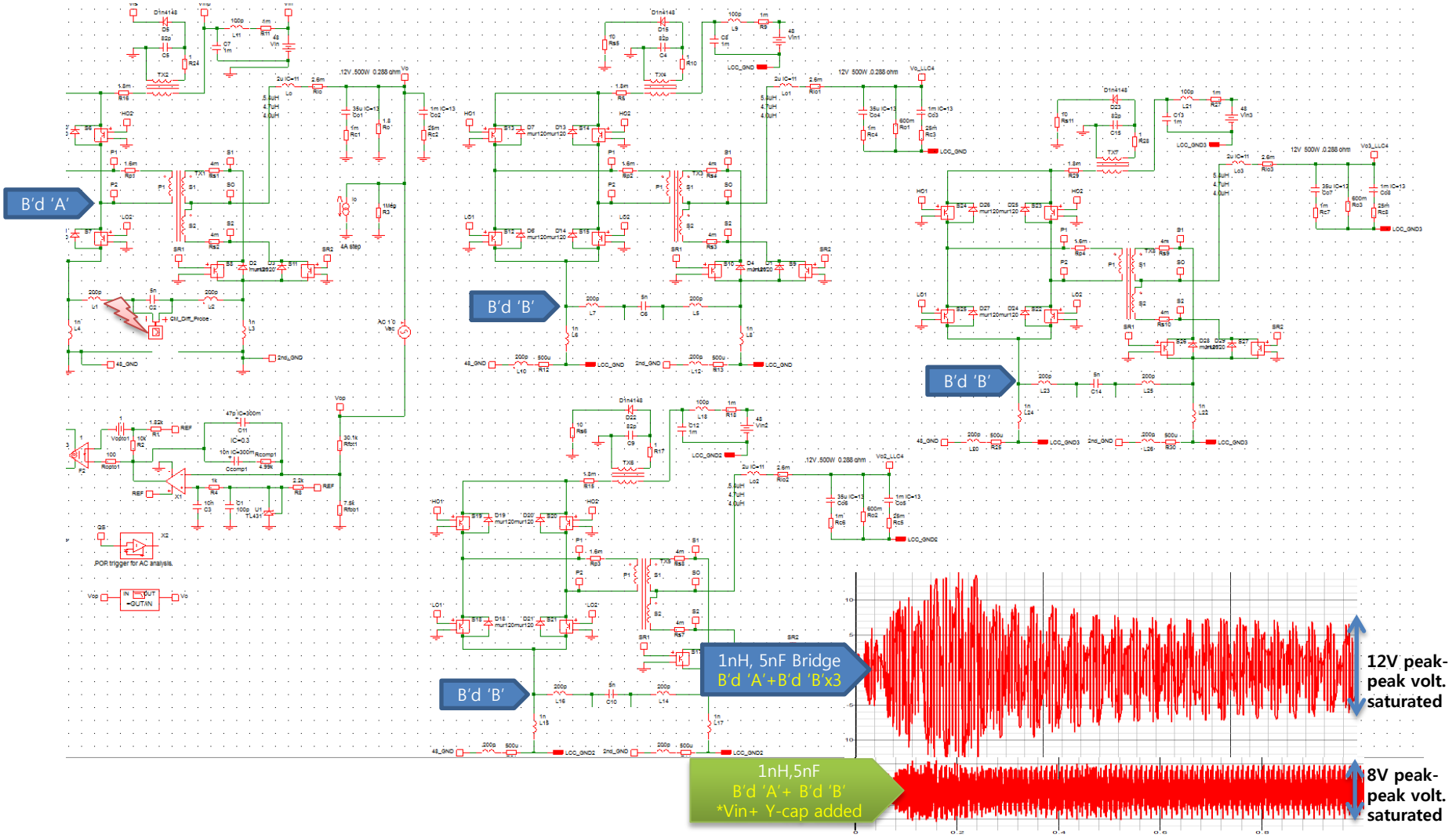
Design guide #1



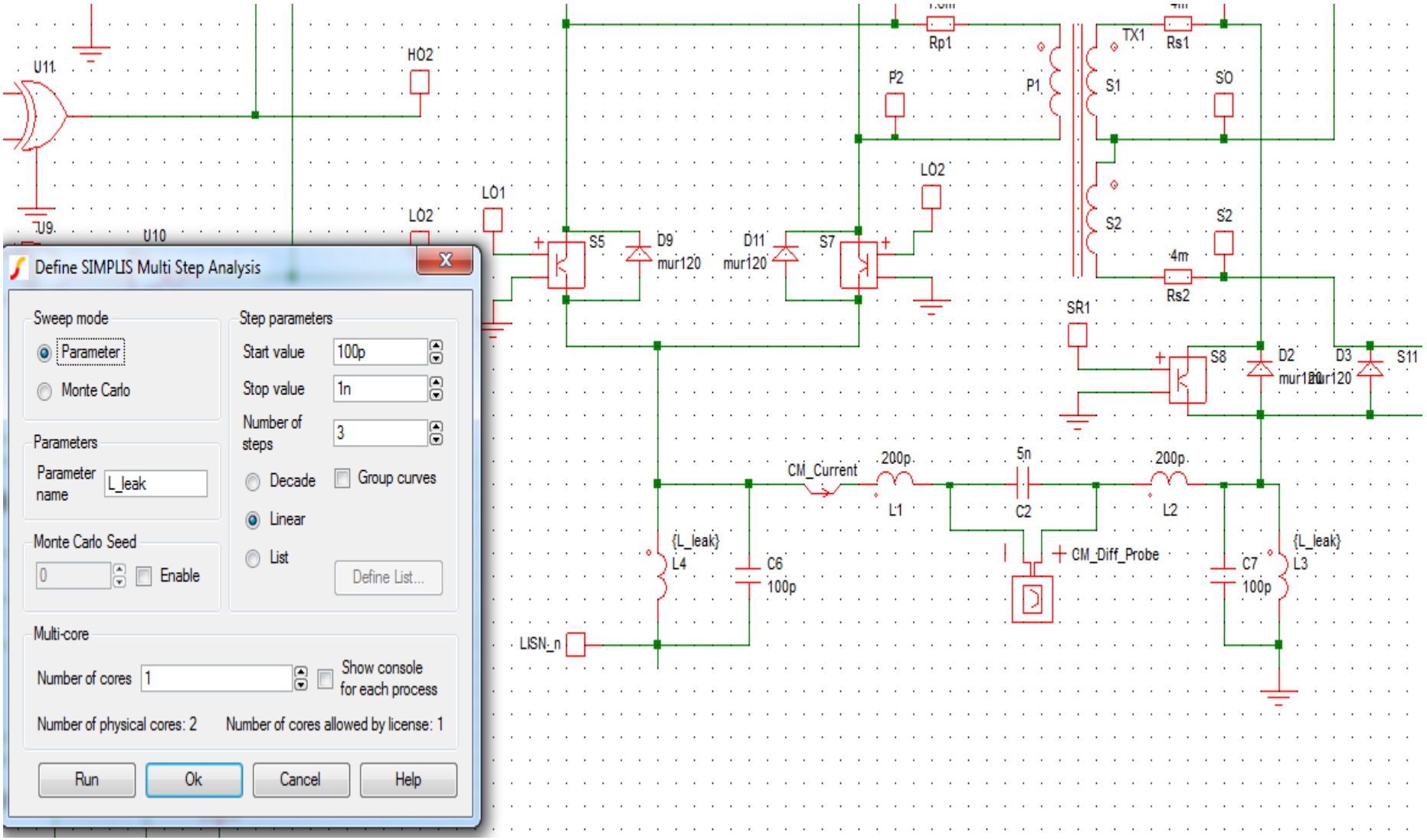


CM 1st~2nd Ground voltage gap Simulation

- Add x3 b'd on the back

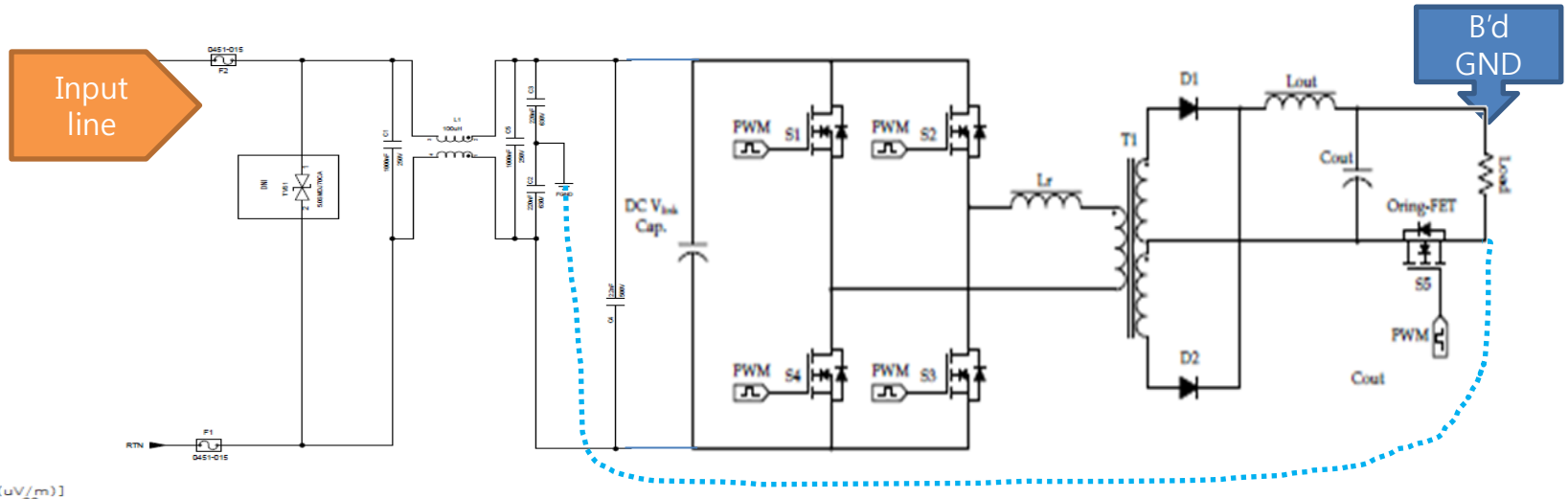


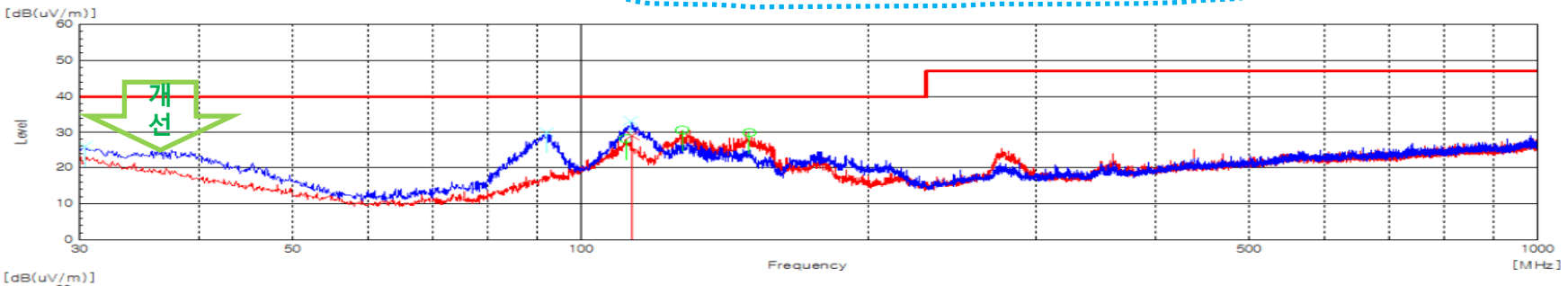
Parameter sweep(Multi-step)

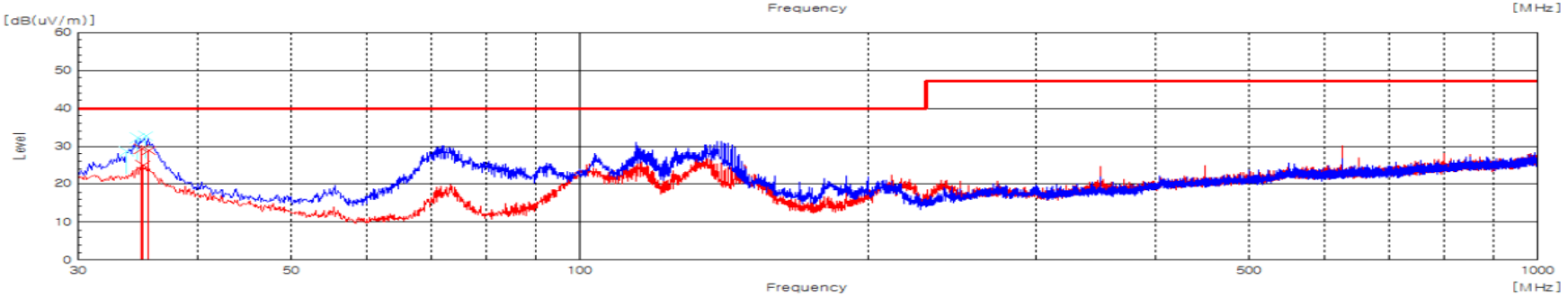


Multi-Sweep result (~x 3 running time)

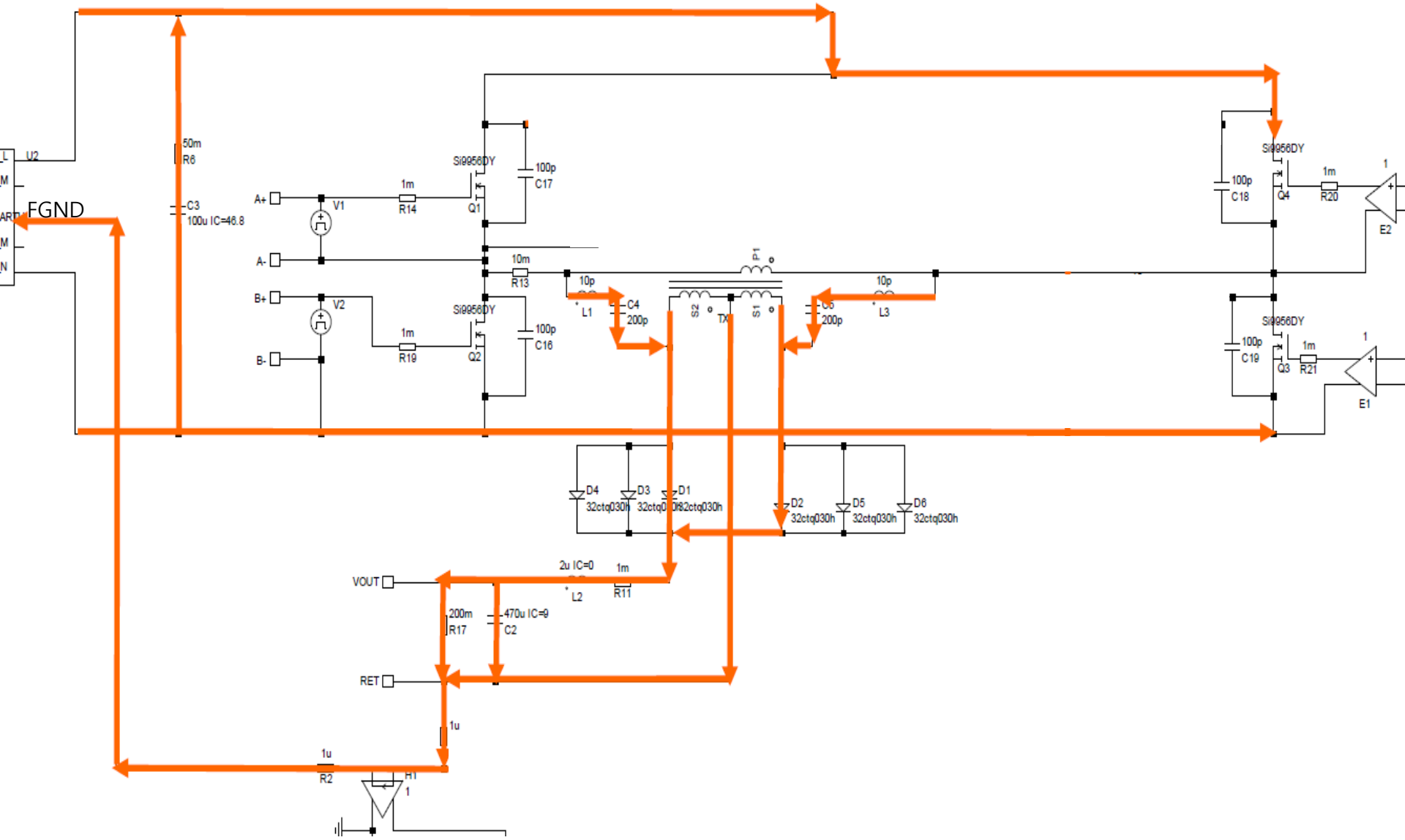
[C.M Current return path]
Intensify the noise sink path



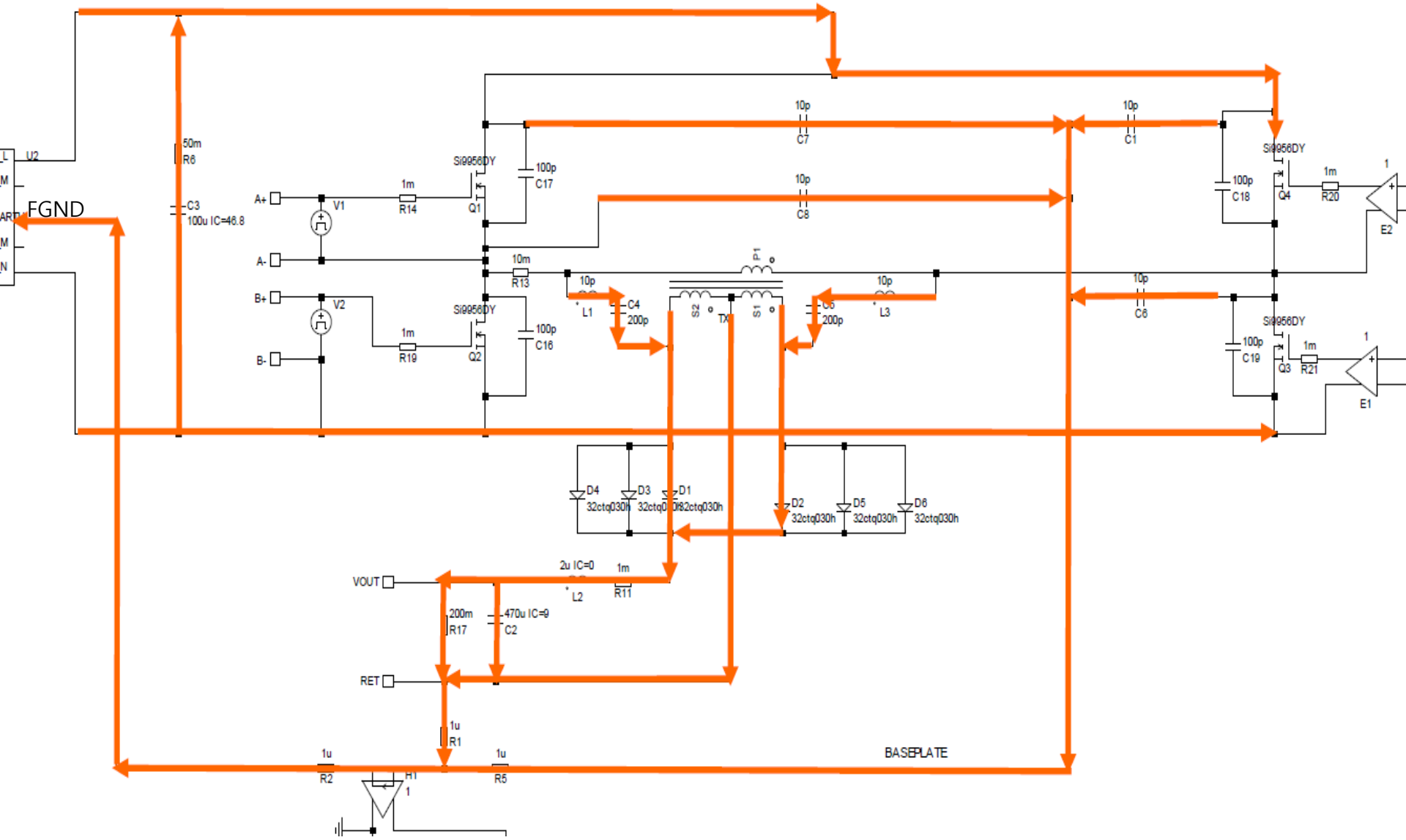




[Appendix 1] Common Mode current Path

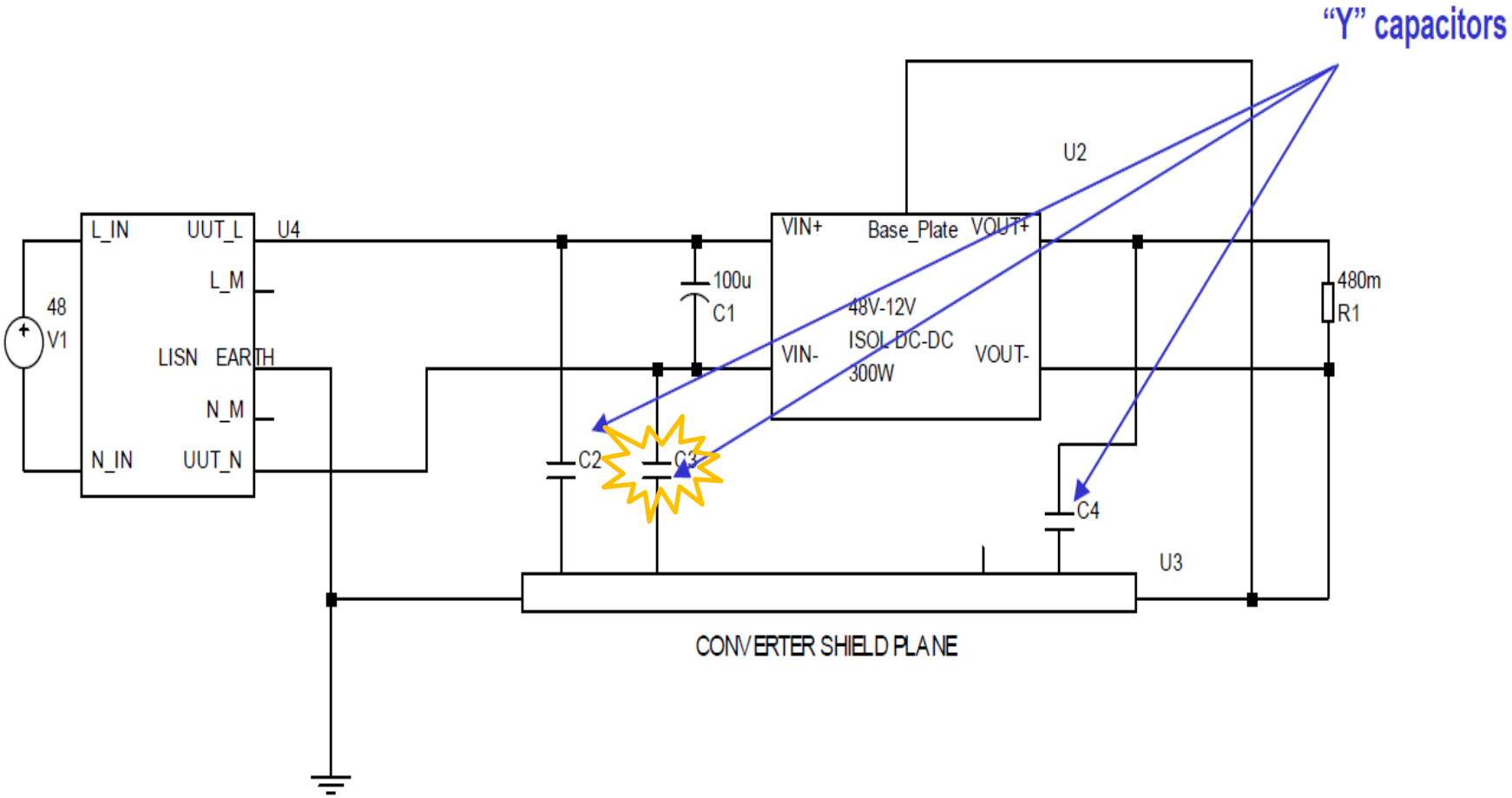


[Appendix 2.1] Common Mode current Path



[Appendix 2.2] Common Mode Y-cap

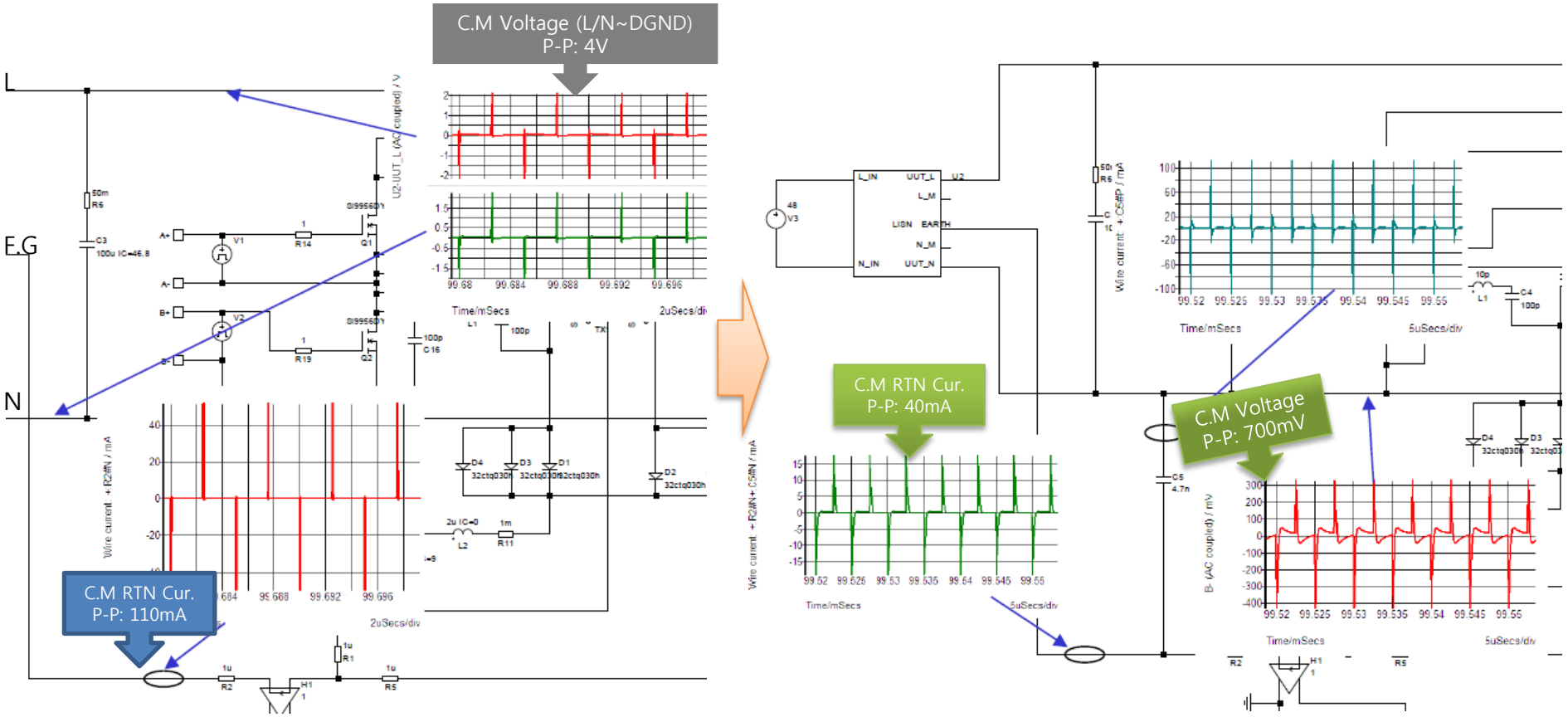
- With Base plate, effective Y-cap position
- "Y" capacitors are added to provide a lower impedance path for current to flow and to reduce the level of common mode voltage that appears between L-N and ground.(Fr. Application note)



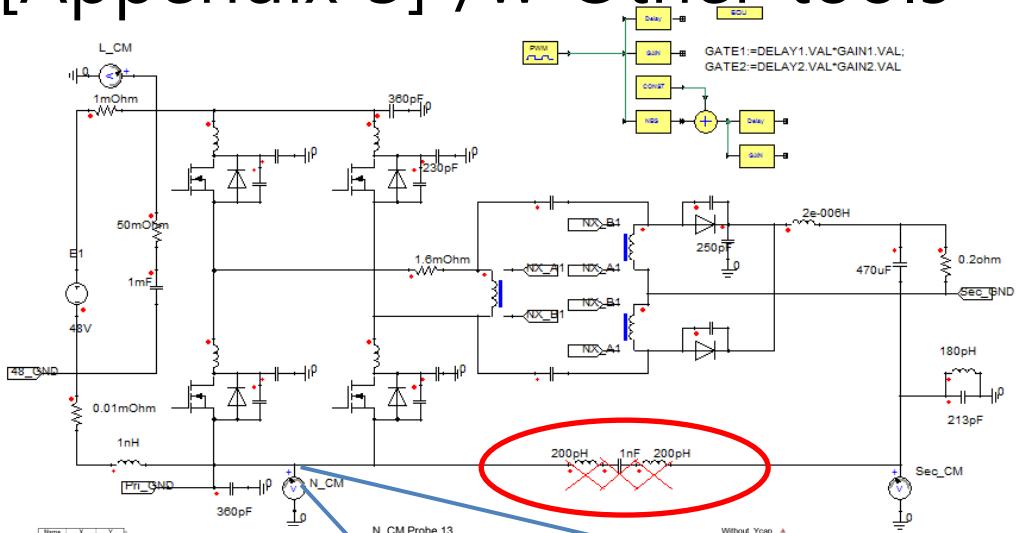
[Appendix 2.3] Common Mode Y-cap effect

- With Base plate, effective Y-cap

→ **With 4700pF capacitor added on C3, CM voltage dropped to 700mV p/p from 4V p/p.**

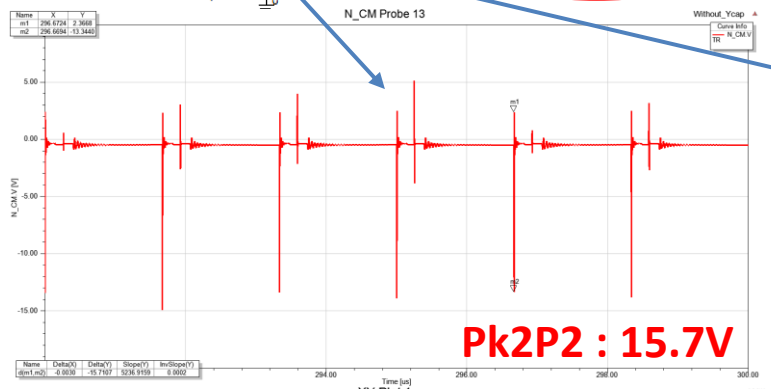


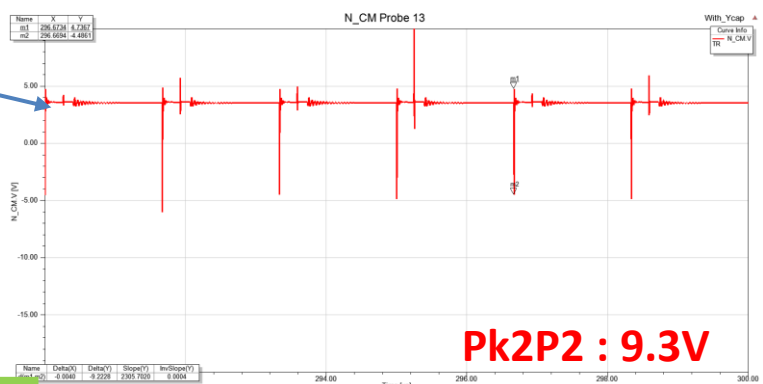
[Appendix 3] /w Other tools



- F.Bridge control

/w C.M parameter change
→ Gain similar Results





FFT