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HFSS를 이용한 Pogo Pin 해석 방법

ANSYS HFSS · SI Technical Note

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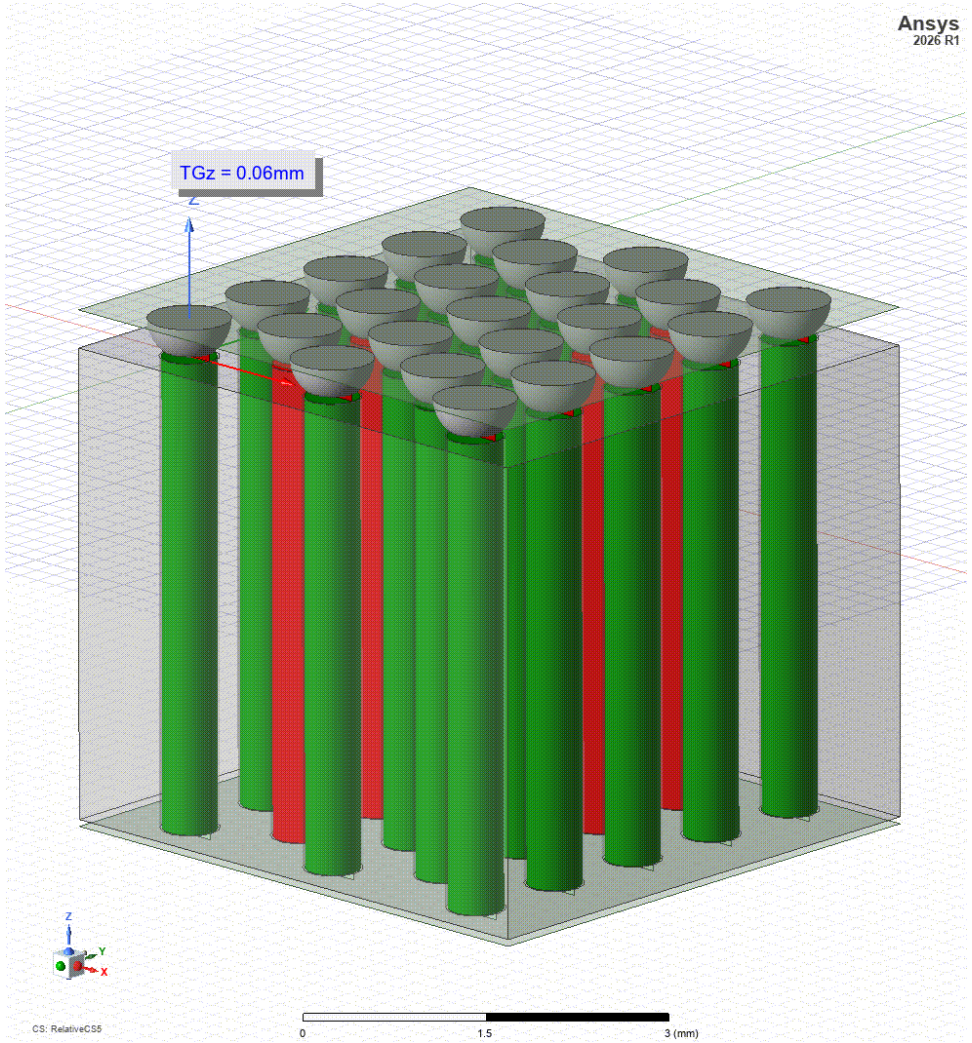
Agenda

- Simulation Condition
- Simulation Check up point : Current Setting related
  - CAD Model Simplification(Plunger, Barrel, Spring)
  - Material setting(Skin effect)
  - Boundary setting (Radiation, Perfect-E, Port)
  - Setup condition(Solution frequency)

- **TDR analysis for checking Lumped port length**
  - Coaxial Lumped port parametric setup
  - Vertical Lumped port parametric setup
  - Proper Port Selection

- **Solder ball + Lumped port setup**
- **Crosstalk & Eye analysis**

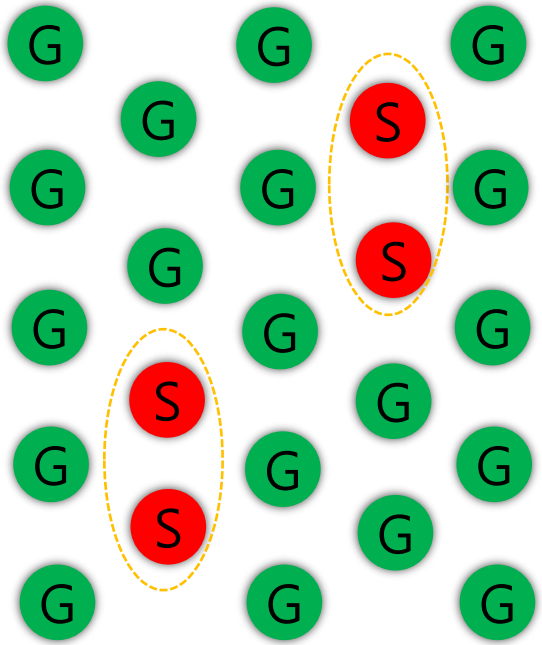


Simulation Condition

Simulation Set up

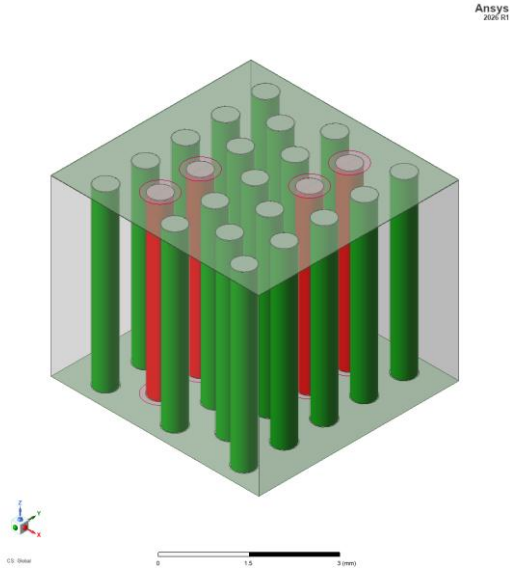
- Simulator : ANSYS HFSS
- Simulation up to 100GHz
  - ✓ 0MHz ~ 100GHz (0.05 GHz Step)
- TDR Set up
  - ✓ Circuit Design
  - ✓ Rise time : 5 ps
  - ✓ Pulse width : 10 us
  - ✓ Pulse repetition : 20 us
  - ✓ Z0 : 85 Ohm
- S-parameter Target (Default)
  - ✓ Insertion Loss > -1.0 dB
  - ✓ Return Loss < -15 dB
  - ✓ Crosstalk < -40 dB

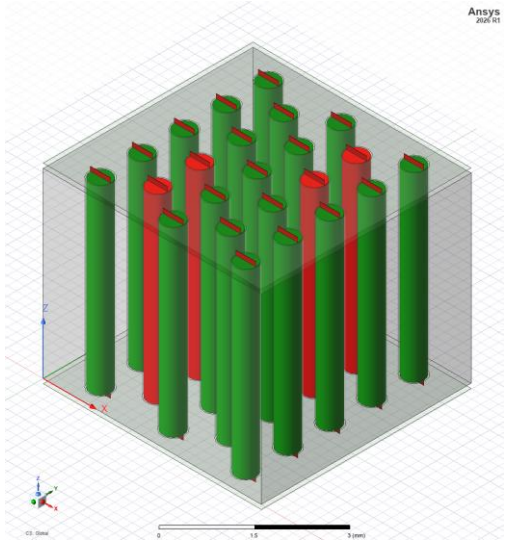
Pin Array 2



Legend

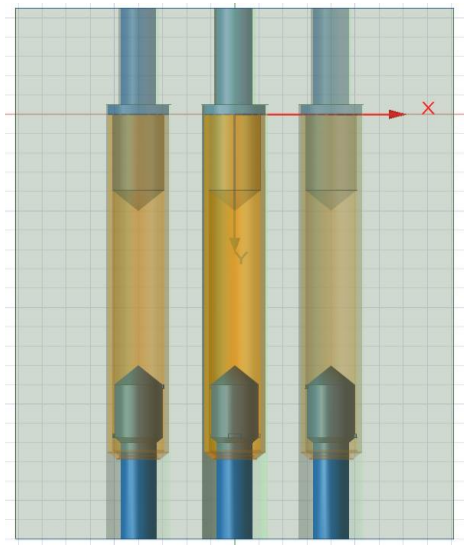
- Signal
- Ground
- Differential Pair

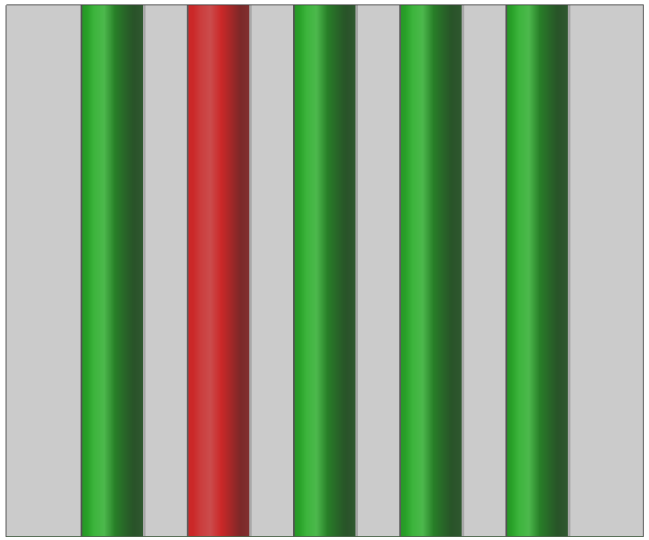




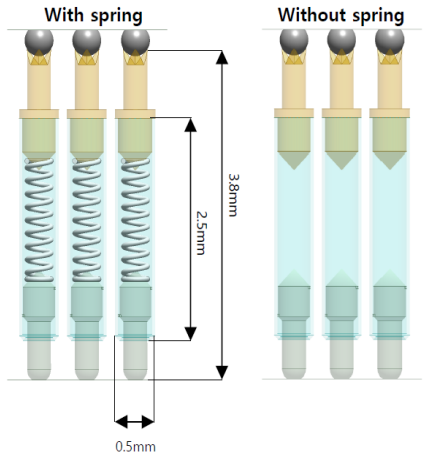
Simulation Check up point

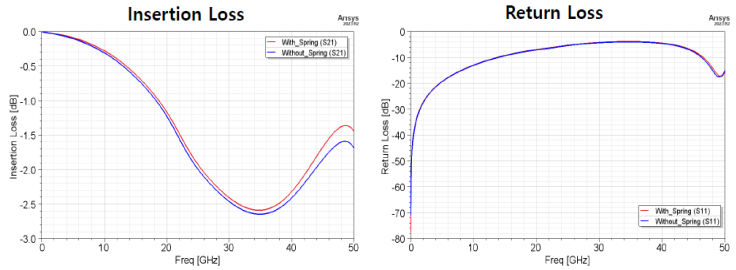
- CAD Model Simplification(Plunger, Barrel, Spring)





◆ Spring 유무에 따른 차이 비교





스프링 유무에 따른 기생성분 분석

	Capacitance[pF]	Inductance[nH]	Solving time
With Spring	0.483	0.787	01:58:57
Without Spring	0.489	0.789	00:05:30

해석의 결과는 큰차이가 없으나 속도는 X21배 차이

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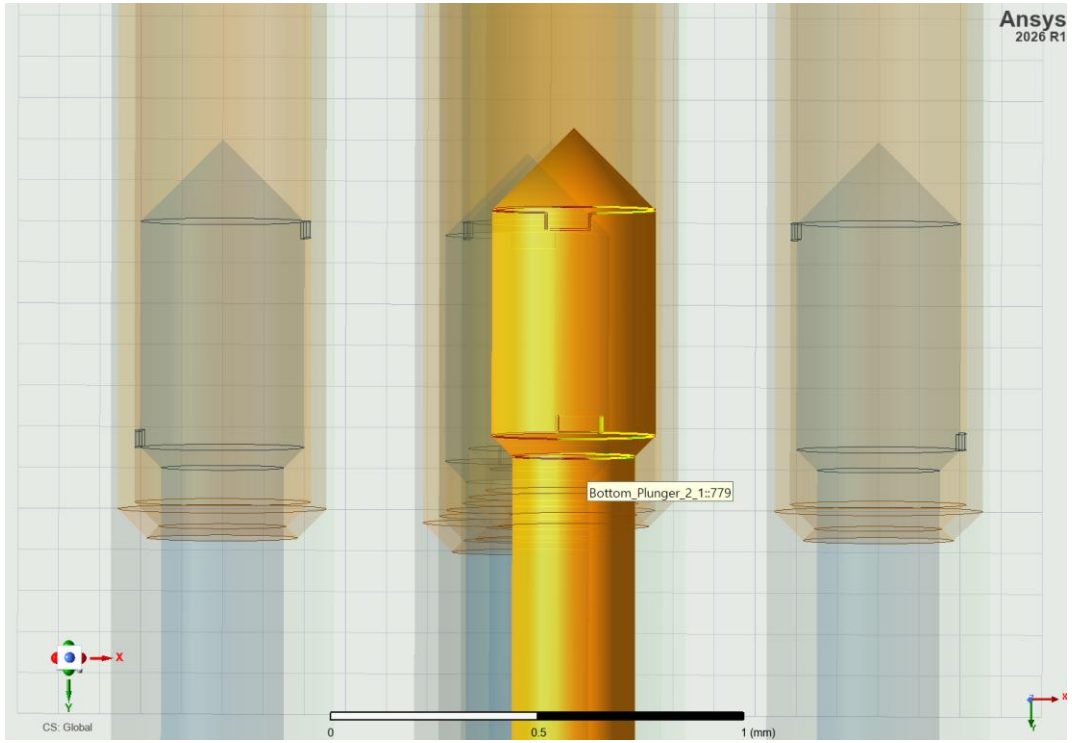
* 2023 TSNE Pogo pin 소켓세미나 발표 자료에서 발췌

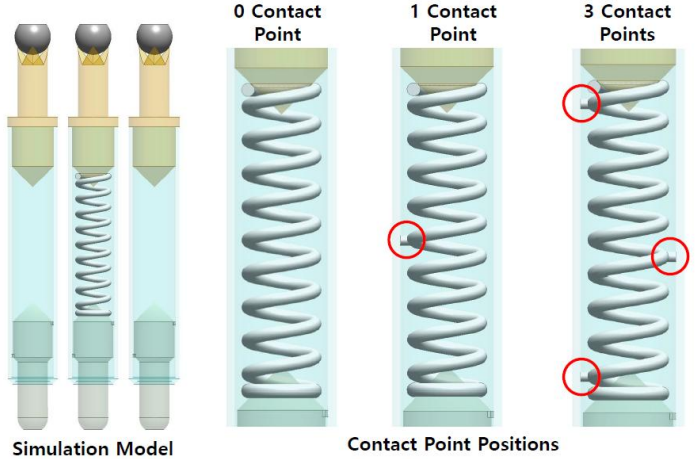
Simulation Check up point

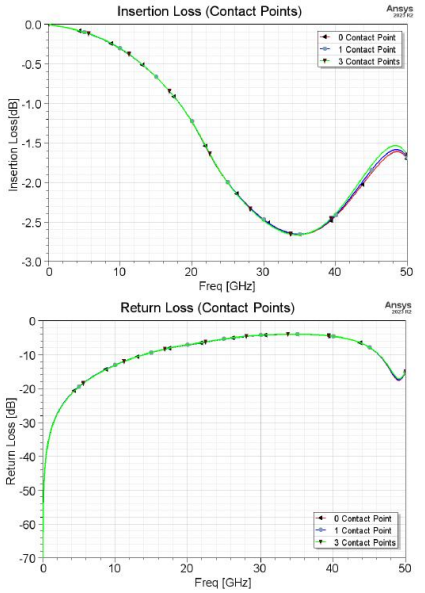
- CAD Model Simplification(Spring contact)



◆ **Spring 접점 차이 비교**

- 현실에서 Spring은 다양한 형태로 눌릴 수 있음 (C자 S자)
- 시뮬레이션에서 눌리는 형태에 따라서 결과 차이가 있는지 비교





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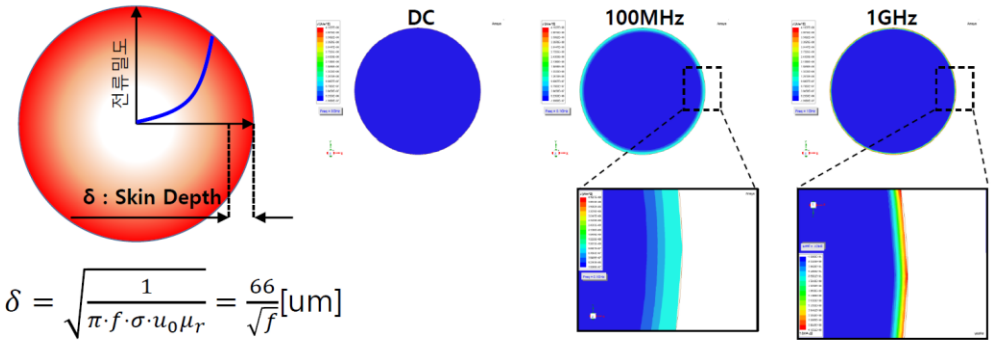
Simulation Check up point

- Material setting(Skin effect)

◆ **표피효과** f : 주파수

- 표피효과는 주파수가 높아 질수록 도체의 표면으로 전류가 흐르는 현상을 의미
- 중심에서 벗어날수록 exp하게 전류밀도가 증가
- 전류가 흐르는 표면 전류에 대해 1/e(약 0.37배)로 감쇠하는 표면 깊이 Skin Depth(δ)라 함



$$\delta = \sqrt{\frac{1}{\pi \cdot f \cdot \sigma \cdot u_0 \mu_r}} = \frac{66}{\sqrt{f}}[\text{um}]$$

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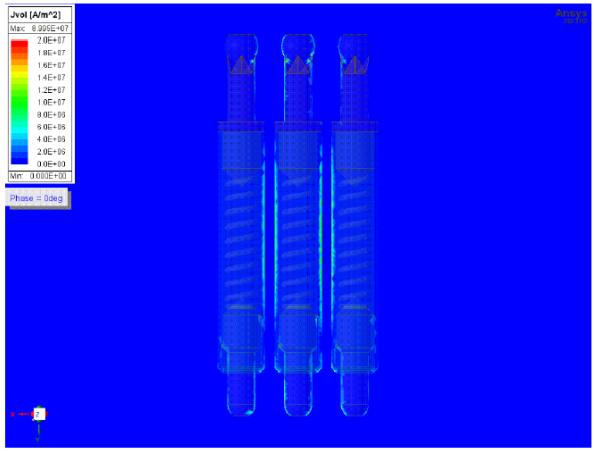
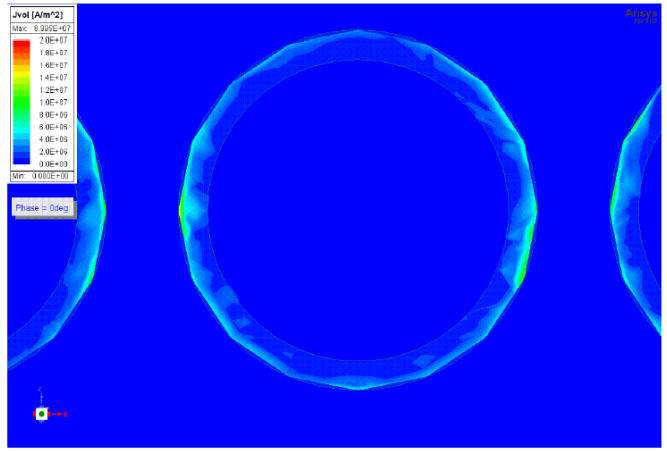
◆ **전류밀도**

- 표피효과에 의해 AC전류에서는 얇은 표면에 대부분의 에너지가 존재
- AC에서는 Spring에는 전류가 흐르지 않음
- 따라서 주파수 해석시 Spring을 제거하고 해석하더라로 결과에 큰 영향을 주지 않음





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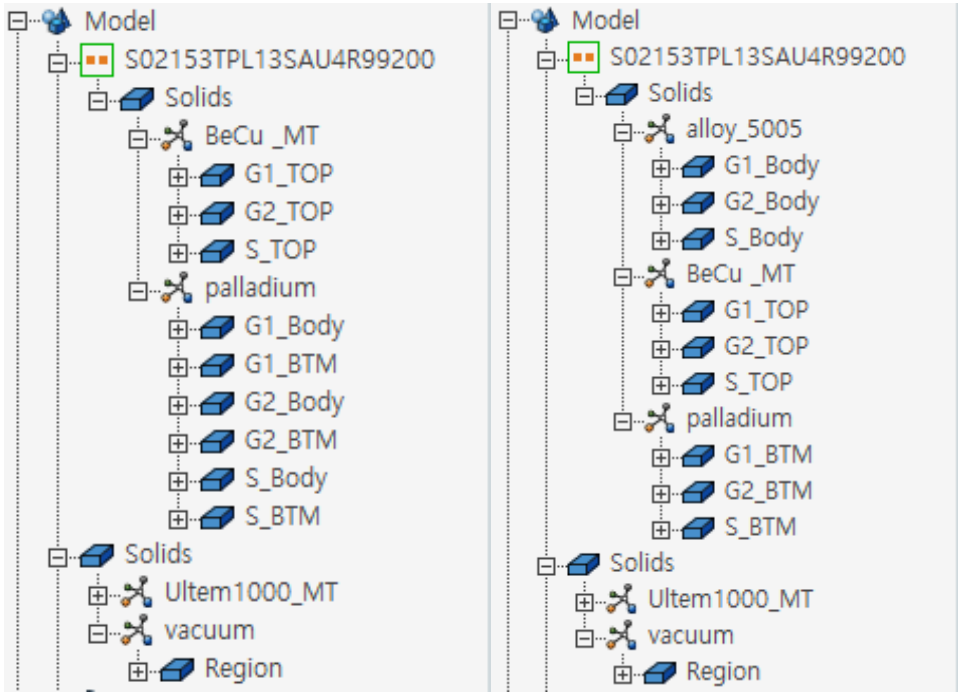
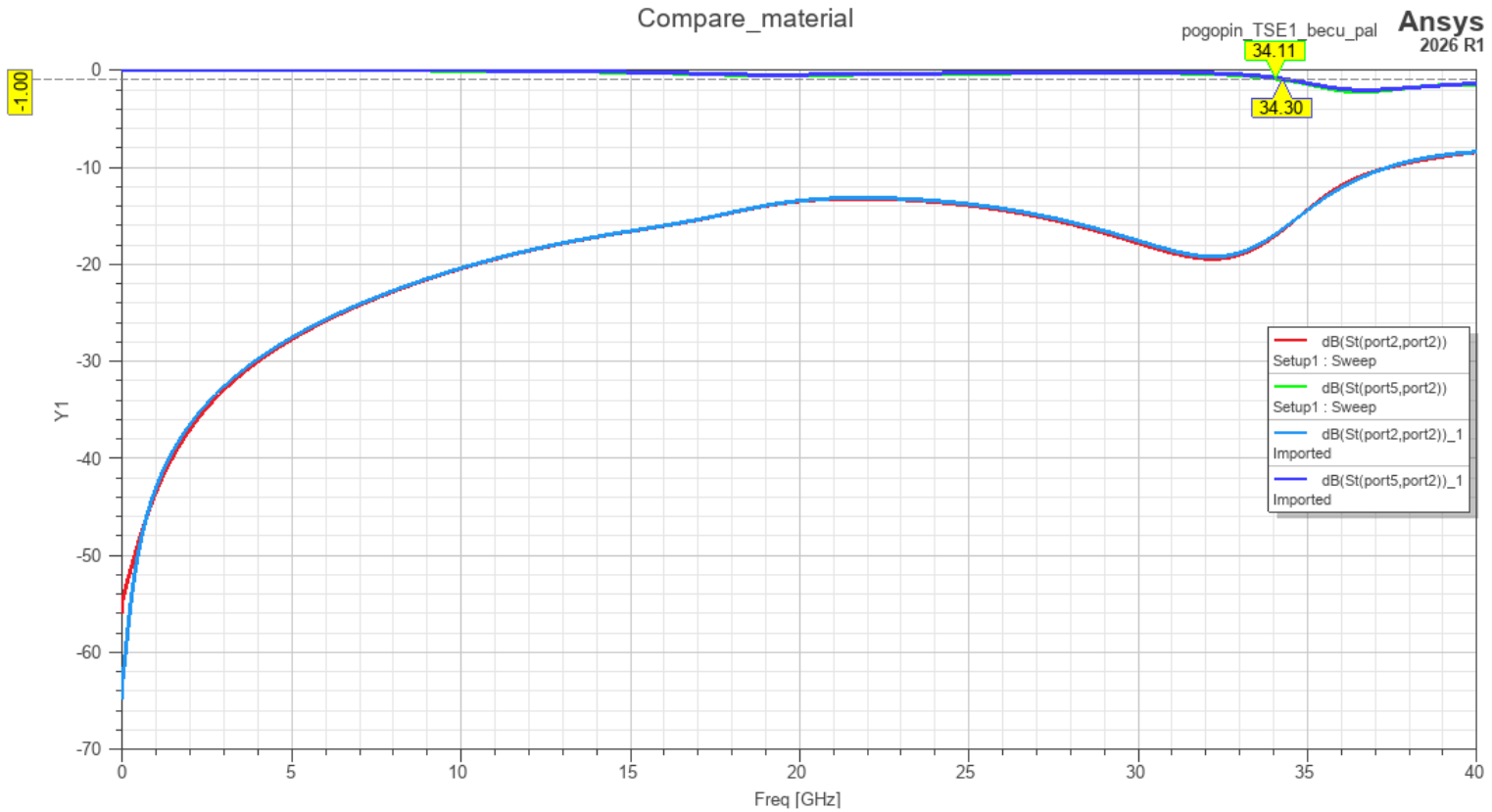
_Becu,_palladium, Alloy5005 의 재질에 대한 Skin effect 특성을 다음장에 나타냄.

Simulation Check up point

- Material setting(Conductor: Skin effect)



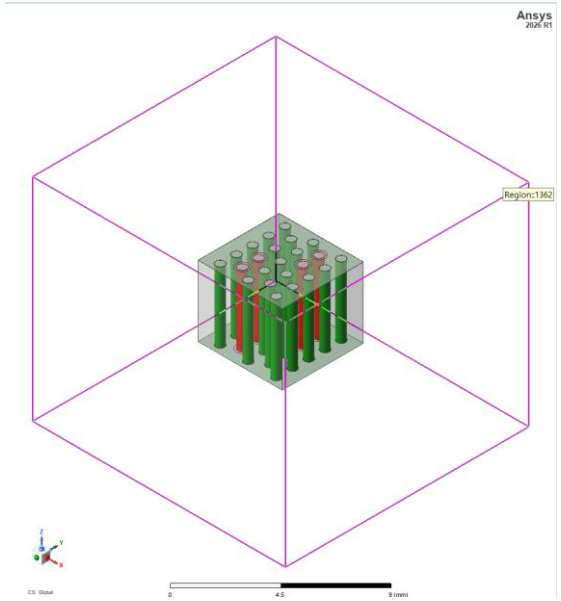


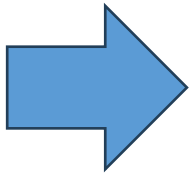
Plunger, Barrel 이 같은 모델에서 재질 설정을 아래와 같이 바꾸었을 때
BeCu, Palladium vs BeCu, Palladium, Aooly_5005

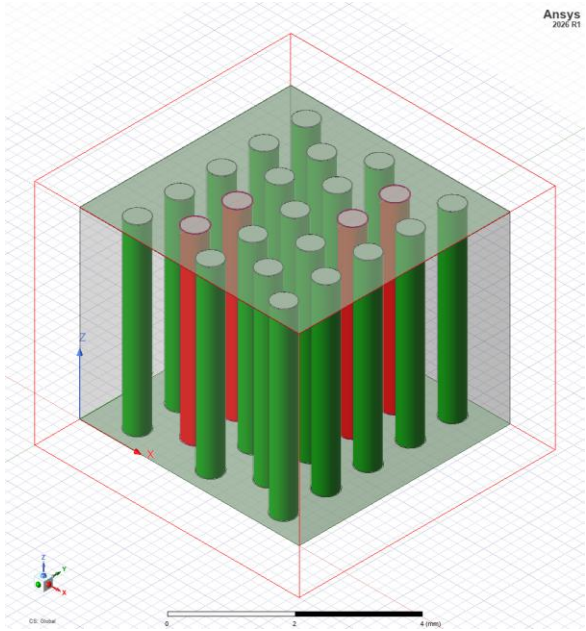
→ S-parameter 결과 거의 동일

Simulation Check up point

- Radiation boundary size : Optimization for Time

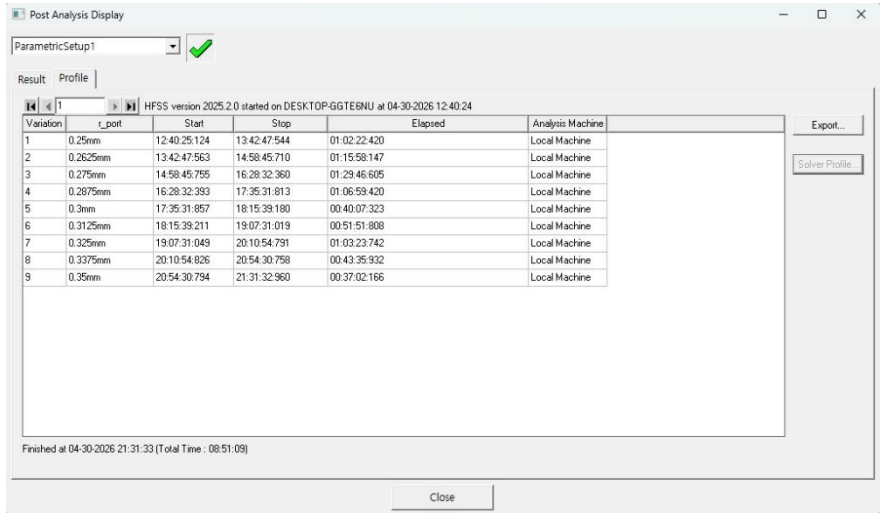


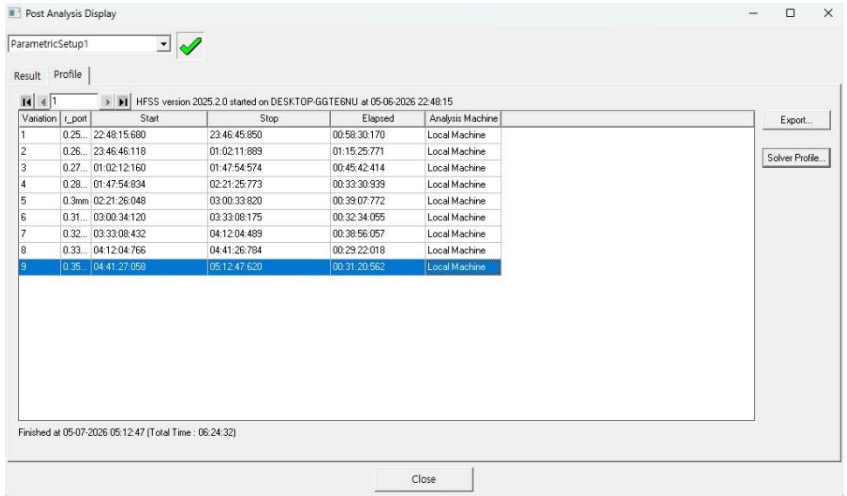




기본적으로 안테나 해석이 아니기에
Radiation boundary 사이즈는 충분히 줄여도 특성 변화 없음.

→ 해석 시간 단축 효과





TDR analysis for checking Lumped port length

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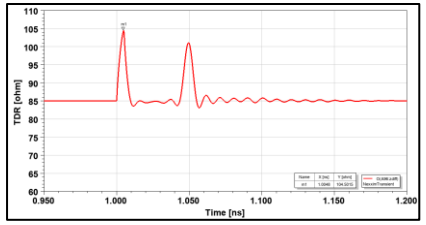
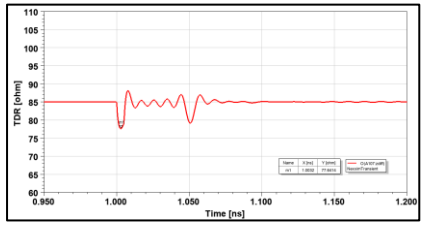
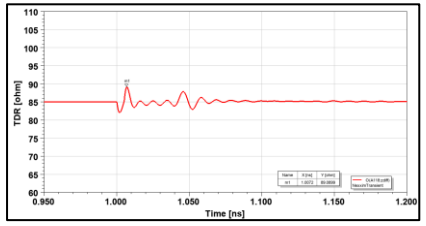
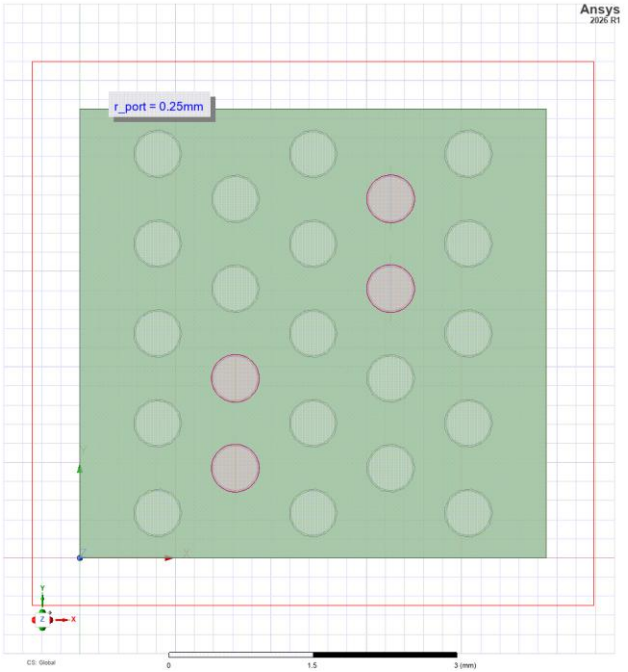
- **TDR 파형으로 Port의 기생성분이 작은 값으로 설정**

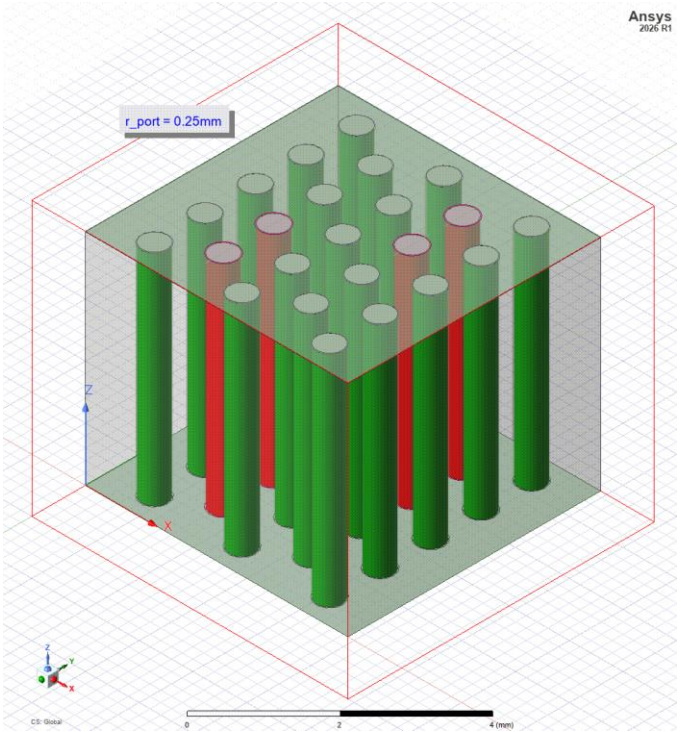
Time Domain Reflectometry 분석은 임피던스 불연속을 시각적으로 보여줍니다. 파형 형태만으로도 포트 길이가 과한지 부족한지 판단 가능함. 이미 예전에 보내주신 자료에 있는 TDR 파형을 그대로 사용하였습니다.

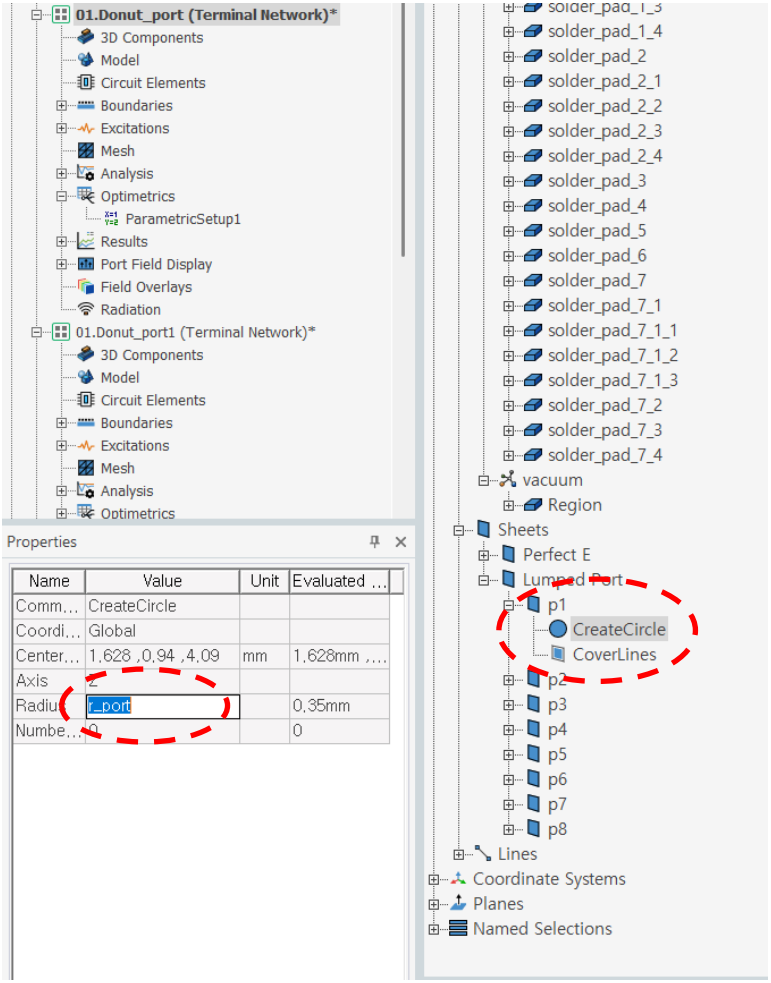
PHENOMENON	TDR WAVEFORM	RECOMMENDED ACTION
Inductive 과다 h 가 너무 김 · L series ↑ Peak ↑ (Z > 85Ω)		**포트 길이 0.2 mm** · 포트 길이 축소 · 또는 De-embedding 으로 직렬 L 제거
Capacitive 과다 h 가 너무 짧음 · C shunt ↑ Dip ↓ (Z < 85Ω)		**포트 길이 0.1 mm** · 포트 길이 증가 · 메쉬 재검토 (종횡비 개선)
양호 적정 길이 + 메쉬 안정 Flat ≈ 85Ω		**포트 길이 0.12 mm** · 현재 설정 유지 · 추후 sweep으로 robust 영역 확정

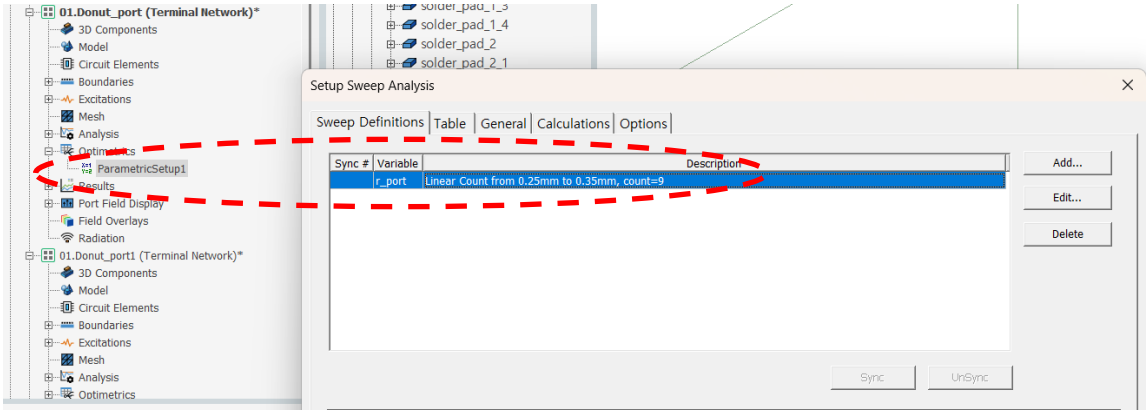
Coaxial Lumped port : Parametric Setup

Coaxial 형태의 Lumped port는 R-port변수를 바꾸어 포트이 사이즈를 증대 시키면 해석을 진행함.



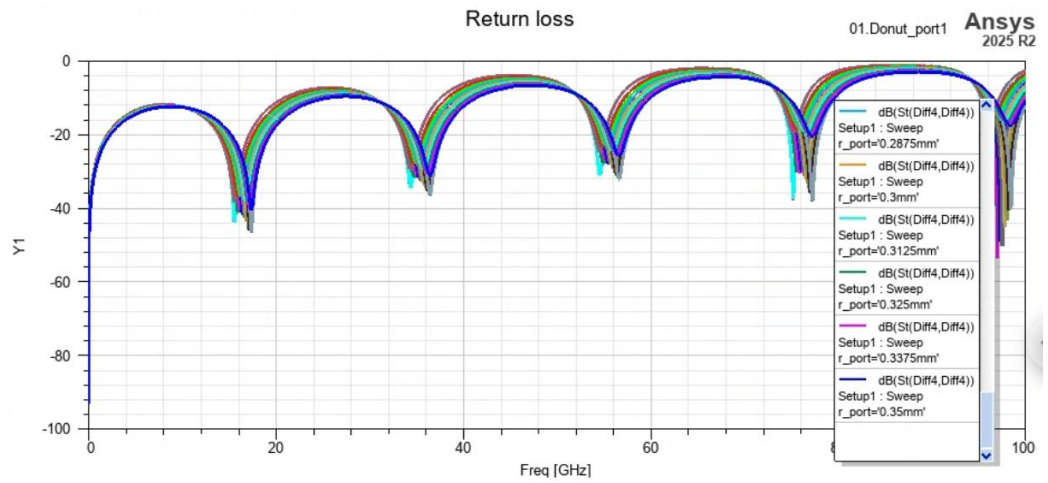


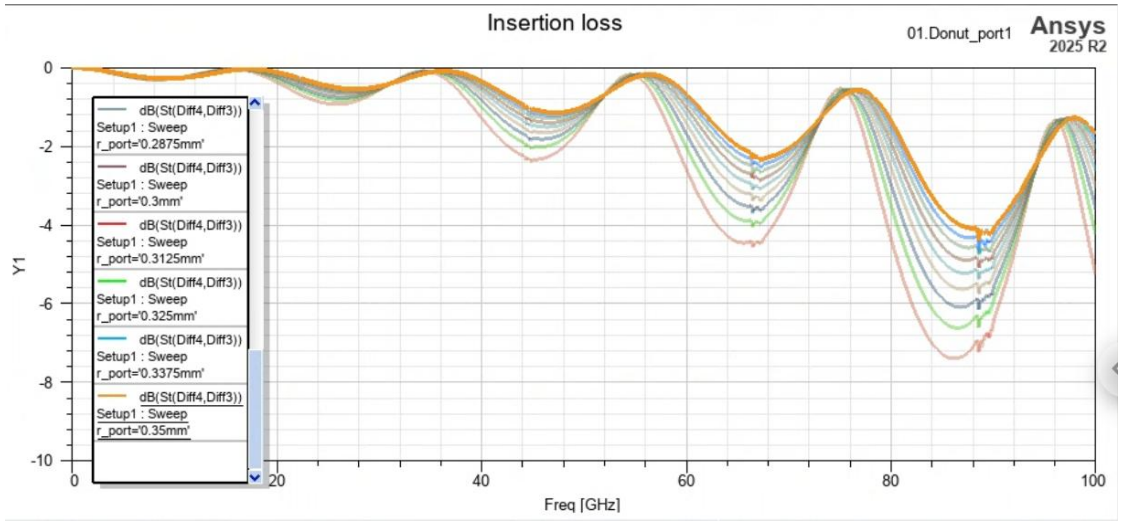


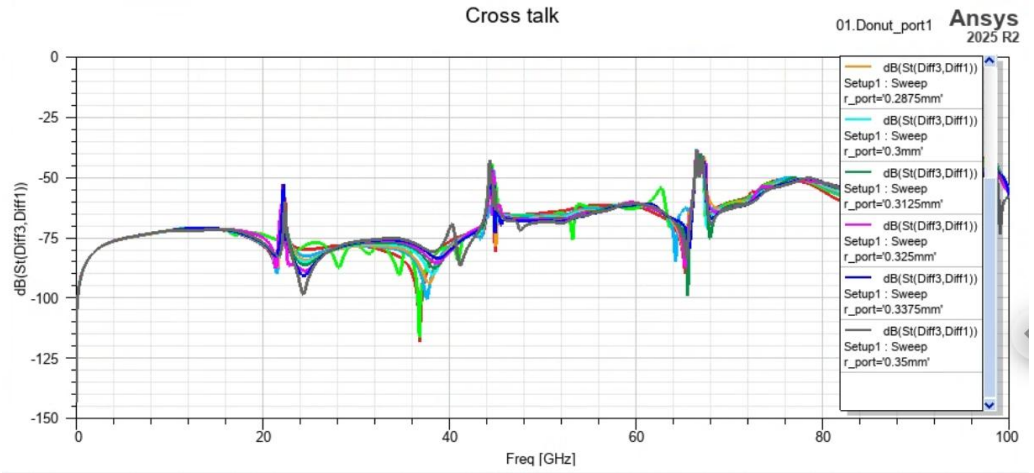


Coaxial Lumped port : Parametric Setup

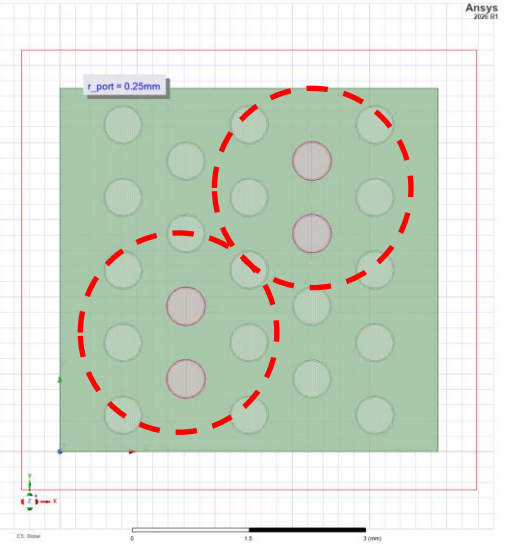
- Return loss, Insertion loss , Crosstalk result



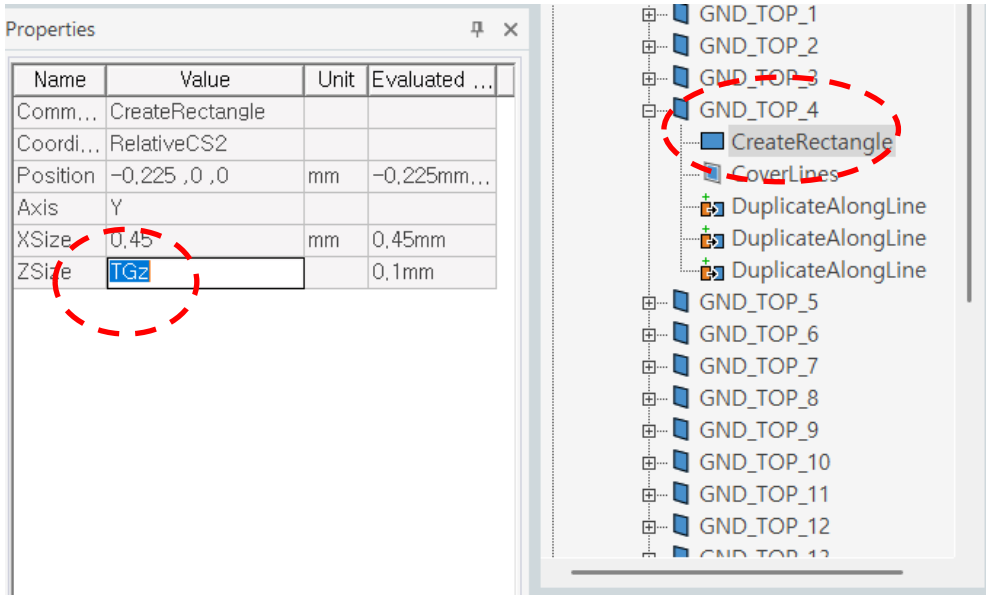


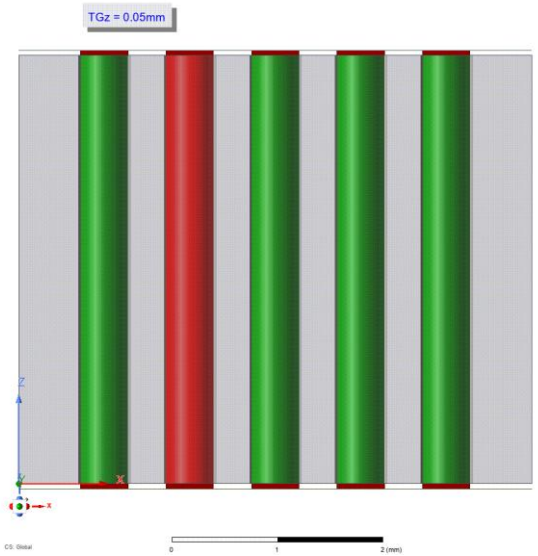


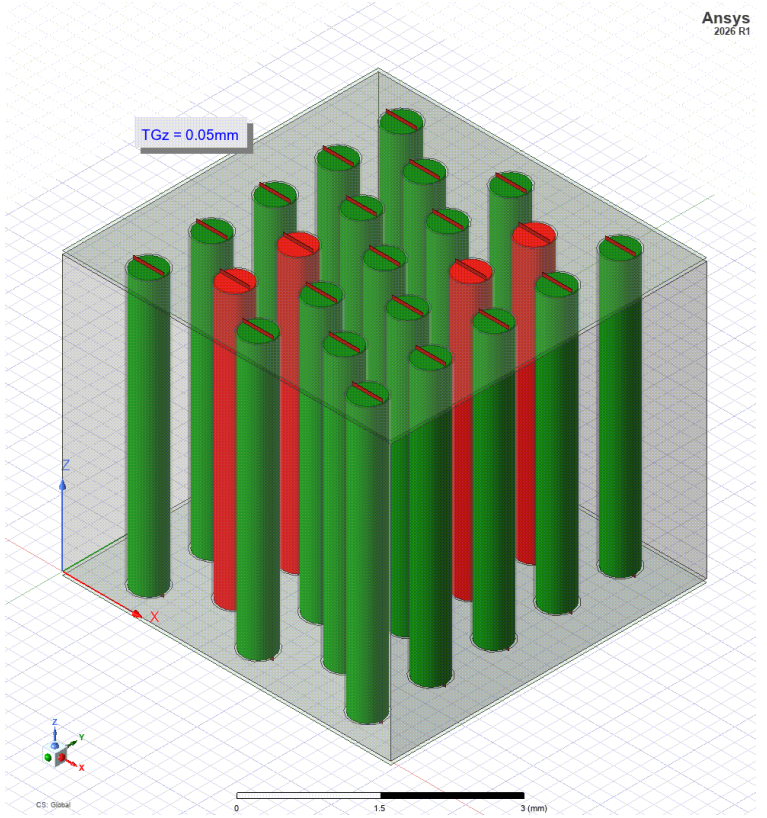
Coaxial 형태의 Lumped port는 Differential pair 인 경우에는 사이즈를 더 키워서 해석 시 포트가 겹치는 부분이 발생하여 해석이 어려움.



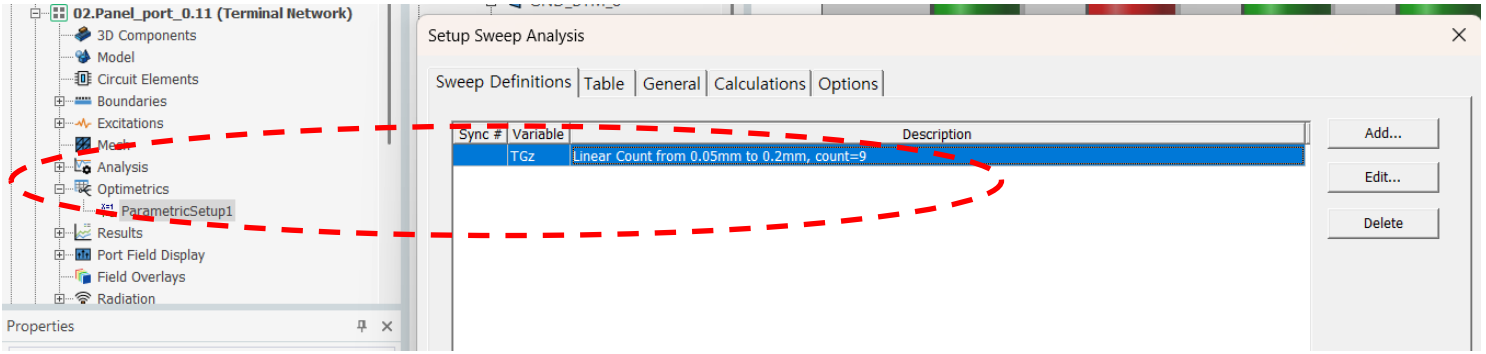
Vertical Lumped port : Parametric Setup





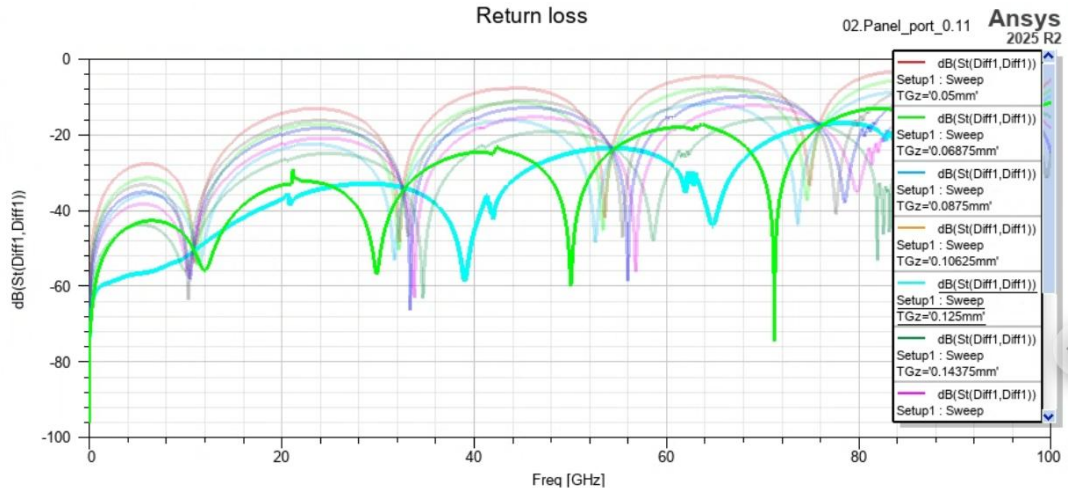


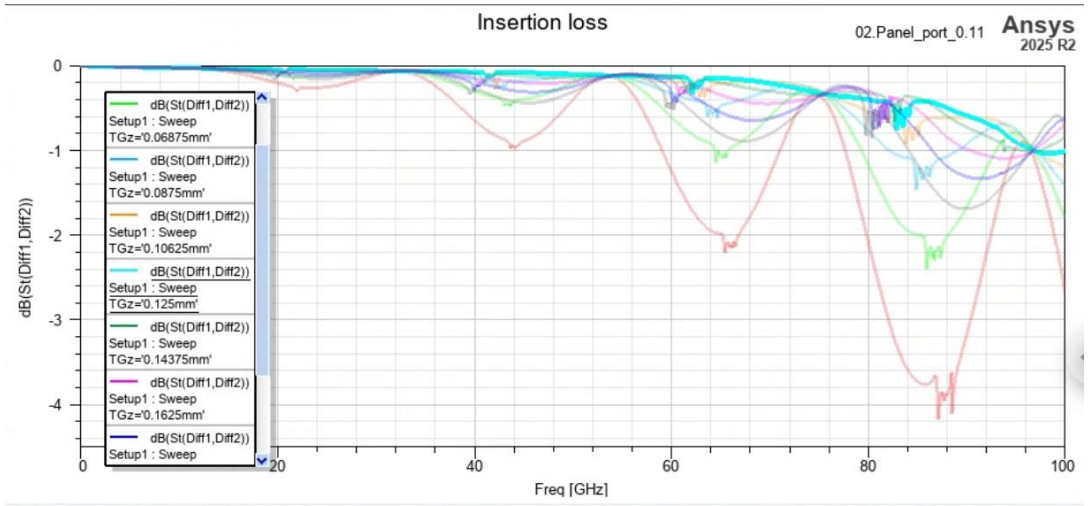
Vertical 형태의 Lumped port는 Differential pair 높이를 변수 TGz로 사이즈를 더 키워서 해석 함.

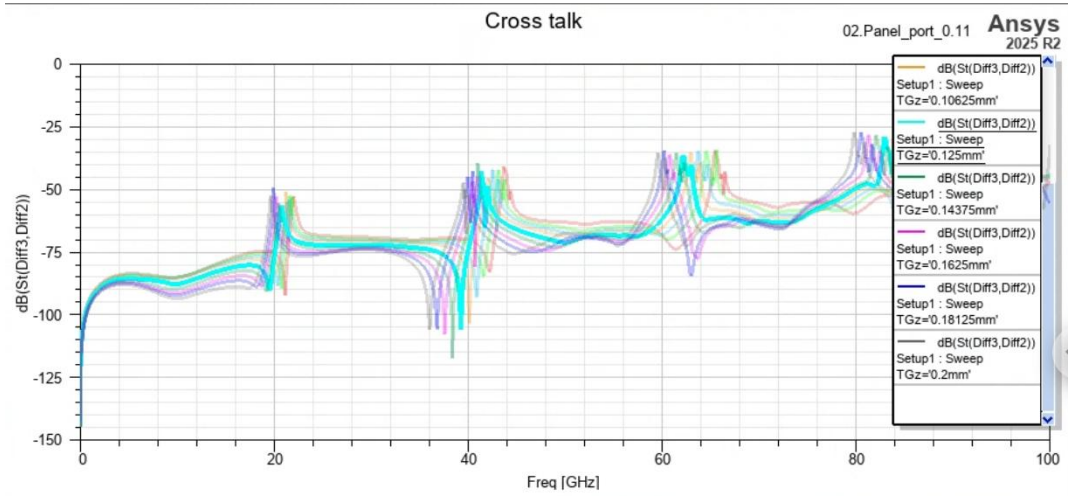


Vertical Lumped port : Parametric Setup

- Return loss, Insertion loss , Crosstalk result







Vertical 형태의 Lumped port는 TGz로 사이즈가 0.125mm 일 때가, 포트의 기생 성분이 최소화된 해석 결과임.

Crosstalk & Eye analysis

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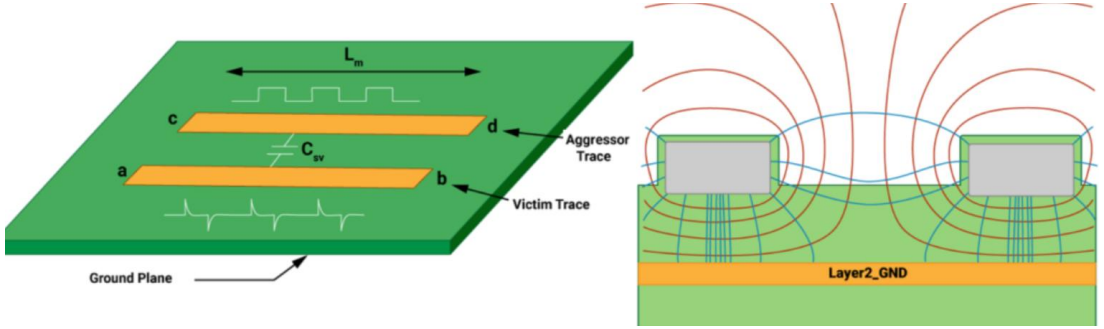
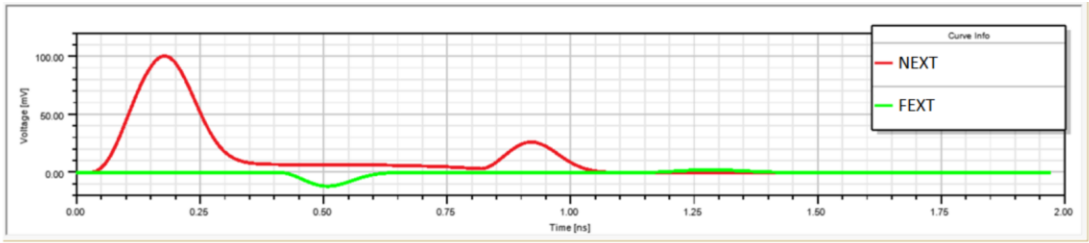
- Return loss, Insertion loss , Crosstalk result

PCIe 배선에서 크로스톡이 발생하는 메커니즘

1. **상호 커패시턴스(C_m) 및 상호 인덕턴스(L_m)**
    1. 신호선(Aggressor)에 급격한 전압/전류 변화($\frac{dV}{dt}$, $\frac{dI}{dt}$)가 생기면 인접한 신호선(Victim)으로 전자기장이 결합하여 원치 않는 노이즈를 유도합니다.
2. **근단 누화(NEXT) vs 원단 누화(FEXT)**
    1. **NEXT (Near-End Crosstalk):** 신호원 방향으로 되돌아오는 노이즈.
    2. **FEXT (Far-End Crosstalk):** 신호 진행 방향(수신단)으로 전달되는 노이즈. PCIe와 같은 스트립라인(Stripline) 및 마이크로스트립(Microstrip) 구조에서 주로 문제됩니다.





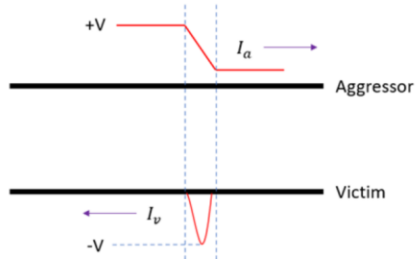
- **간격 확보 (3W / 5W Rule):** 인접한 PCIe 차동 쌍 사이의 간격을 트레이스 폭(W)의 최소 3배~5배 이상 이격시킵니다.
- **GND 가드 및 비아(Via Shielding):** 차동 쌍 사이에 접지 패턴(Ground Guard Trace)이나 스티칭 비아(GND Stitching Vias)를 배치해 결합 전자기장을 차단합니다.
- **스트립라인(내층 배선) 활용:** 위아래로 연속된 그라운드 플레인이 존재하는 내부 레이어(Stripline)에 배선하여 FEXT를 최소화합니다.

Inductive:

$$V_c = -L_M \frac{dI_A}{dt}, I_c = \frac{V_c}{Z_0}$$

Capacitive:

$$I_c = C_M \frac{dV_A}{dt}, V_c = I_c Z_0$$



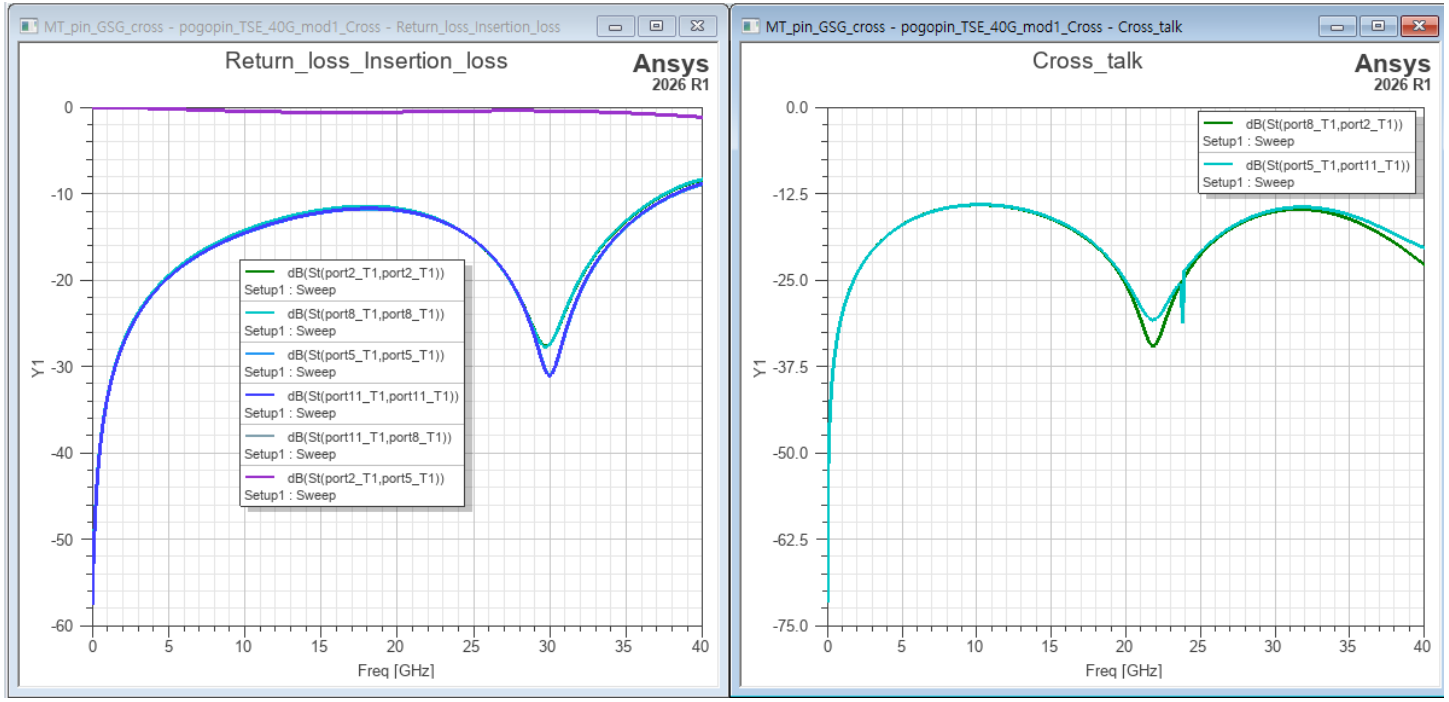
$$NEXT = \frac{1}{4} \cdot \left(\frac{length}{vel \cdot t_{rise}}\right) \cdot \left(\frac{C_M}{C_L} + \frac{L_M}{L_L}\right)$$

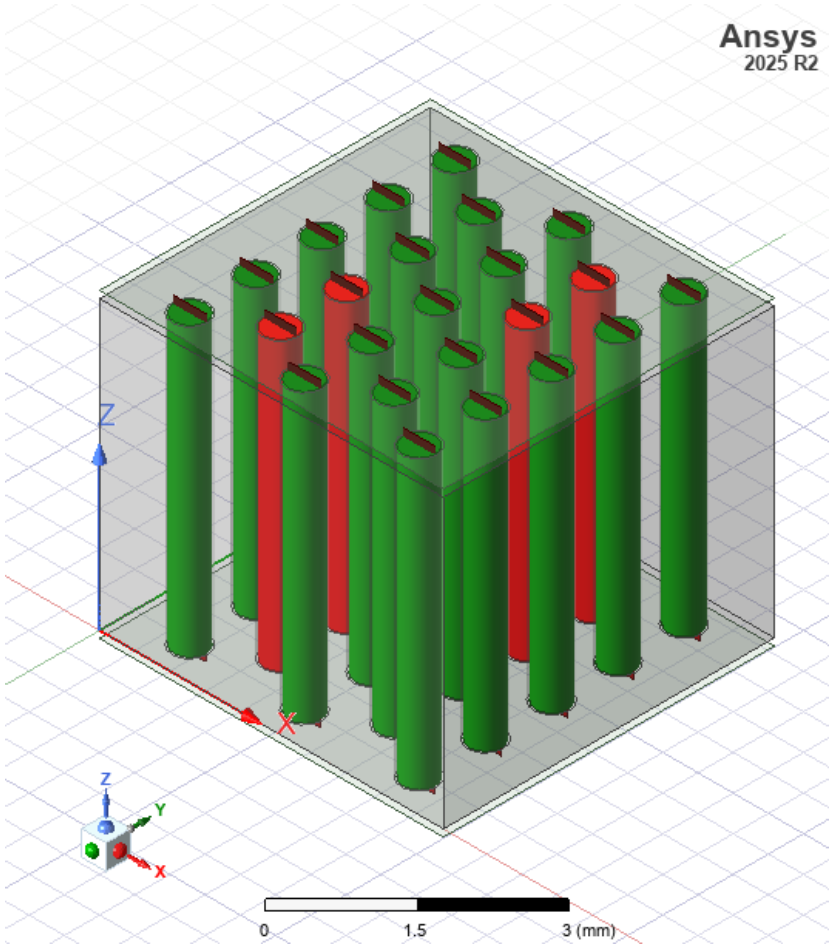
This fraction ≤ 1

$$FEXT = \frac{1}{2} \cdot \left(\frac{length}{vel \cdot t_{rise}}\right) \cdot \left(\frac{C_M}{C_L} - \frac{L_M}{L_L}\right)$$

Crosstalk & Eye analysis

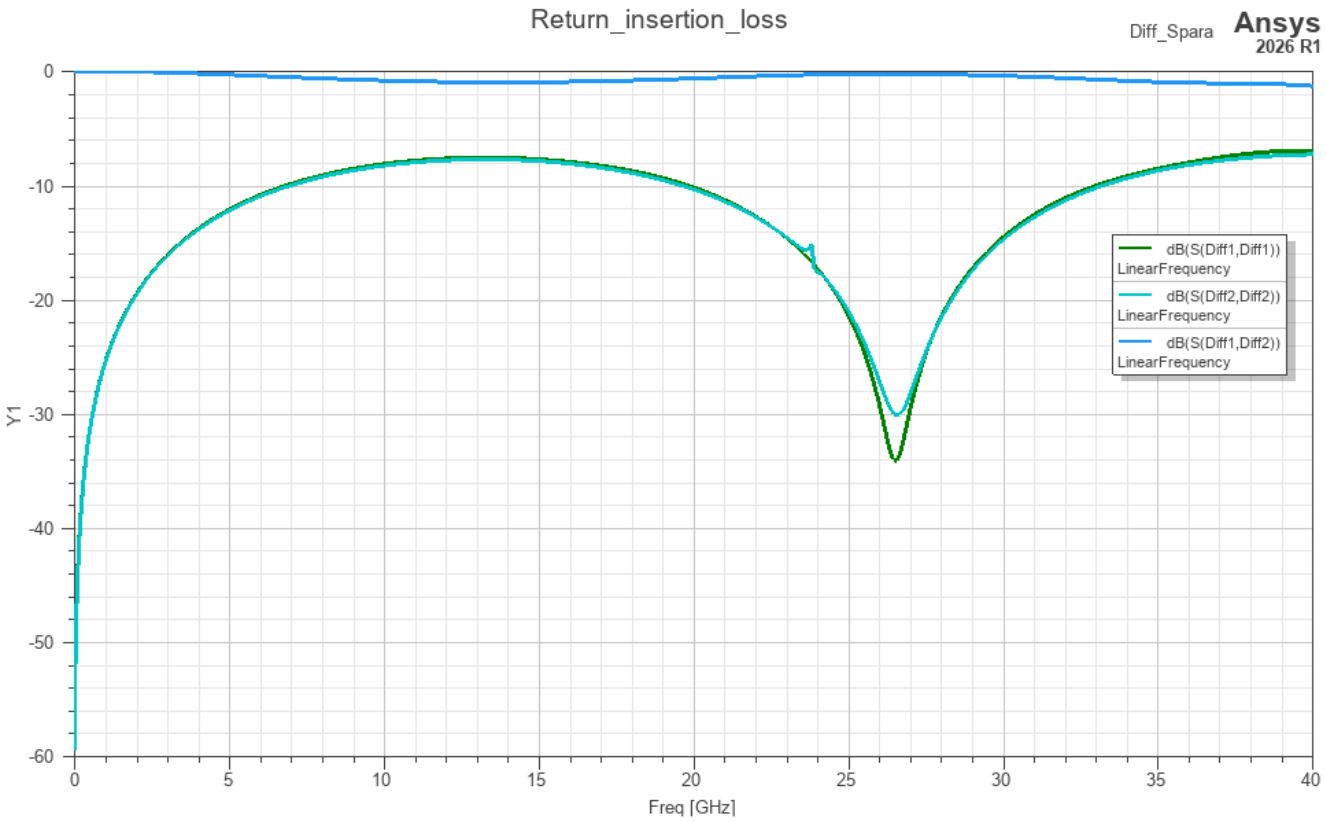
- Return loss, Insertion loss , Crosstalk result



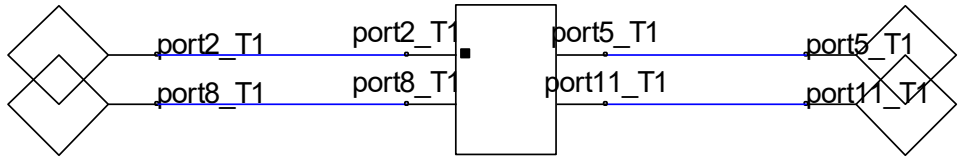


Crosstalk & Eye analysis

- Differential pair S-parameter



32GTps Diff Spara

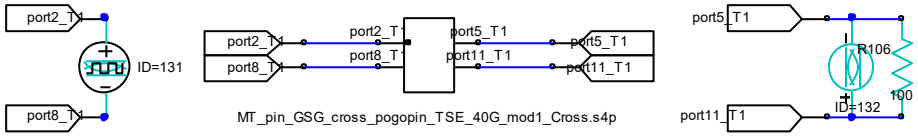


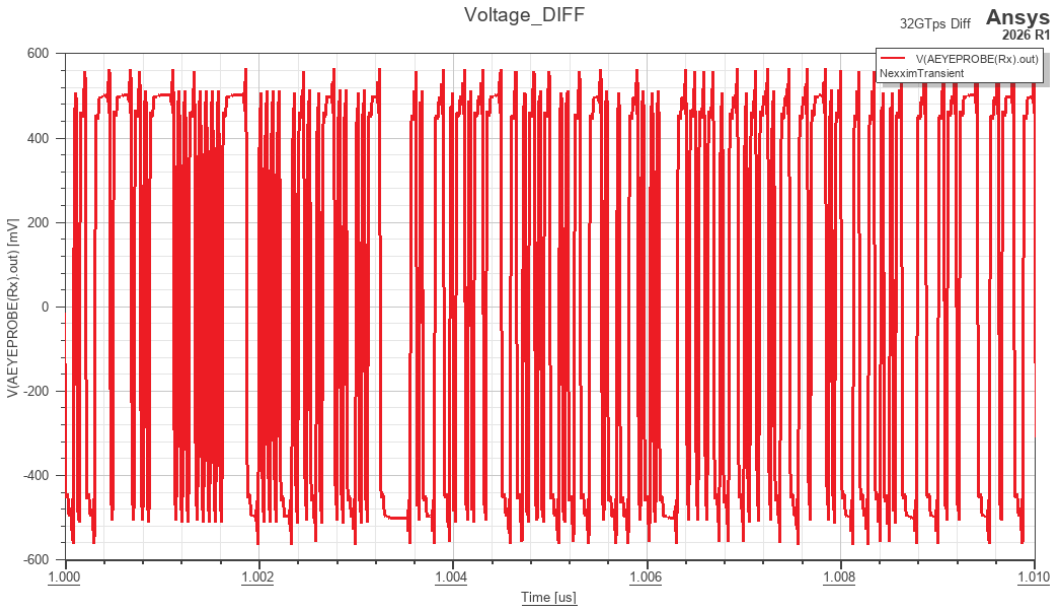
MT_pin_GSG_cross_pogopin_TSE_40G_mod1_Cross.s4p

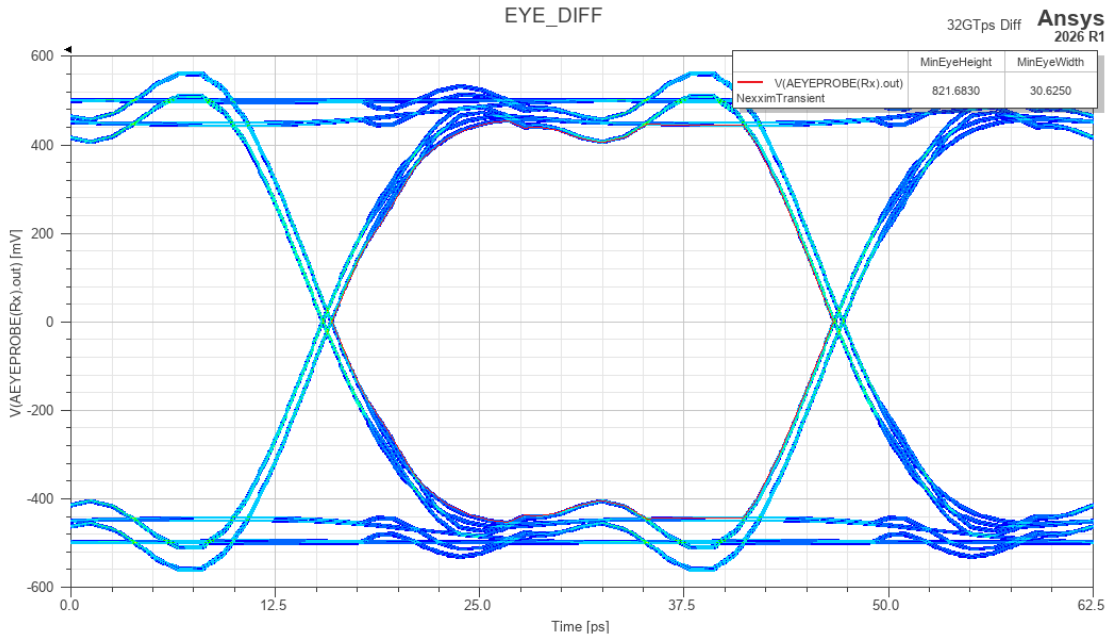
Crosstalk & Eye analysis

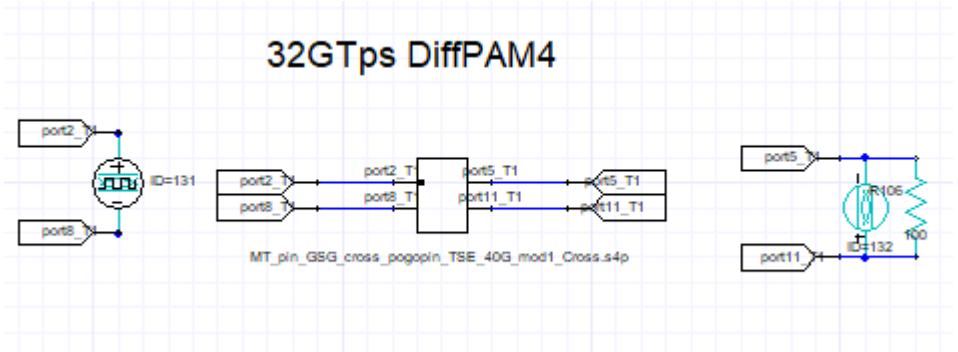
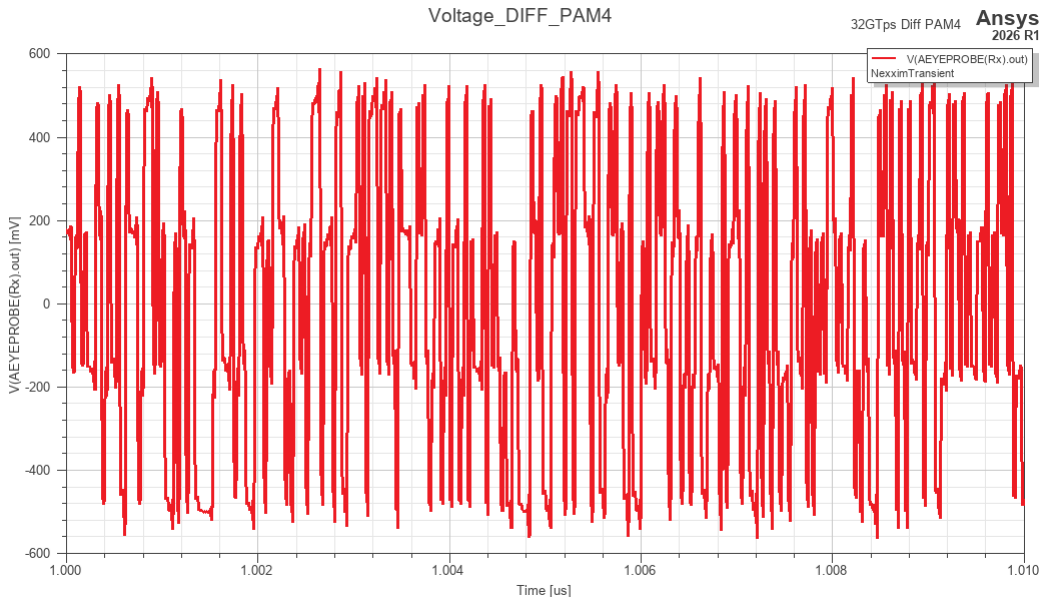
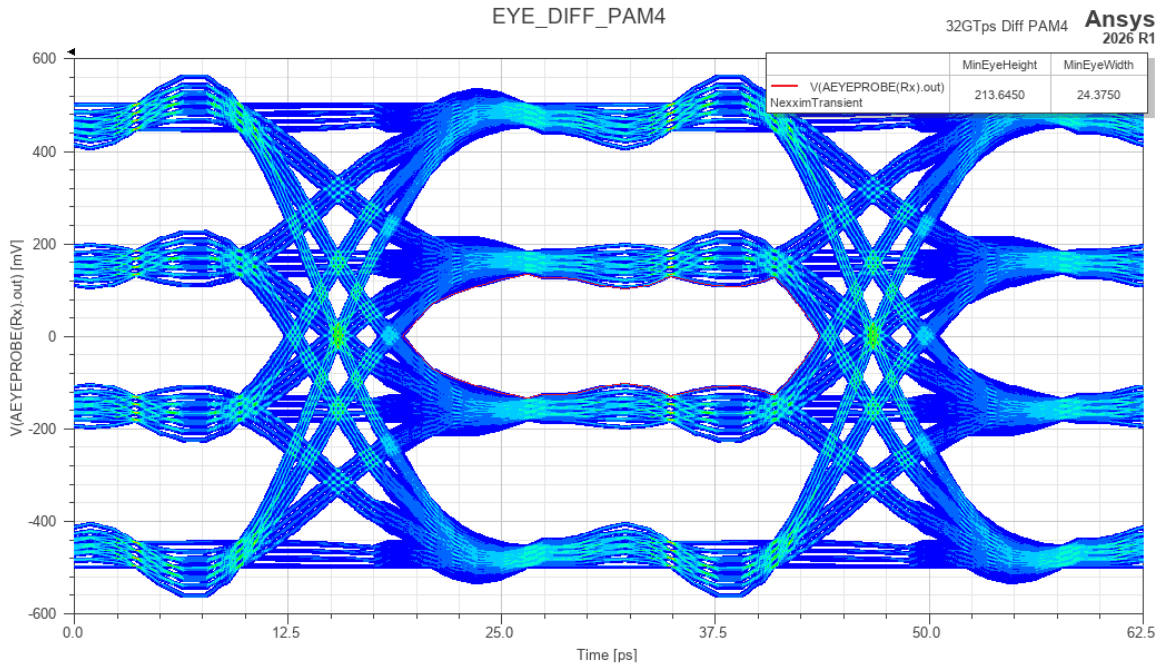
- Differential pair EYE (32Gbps)

32GTps Diff EYE







Crosstalk & Eye analysis

- Differential pair EYE (PAM4)